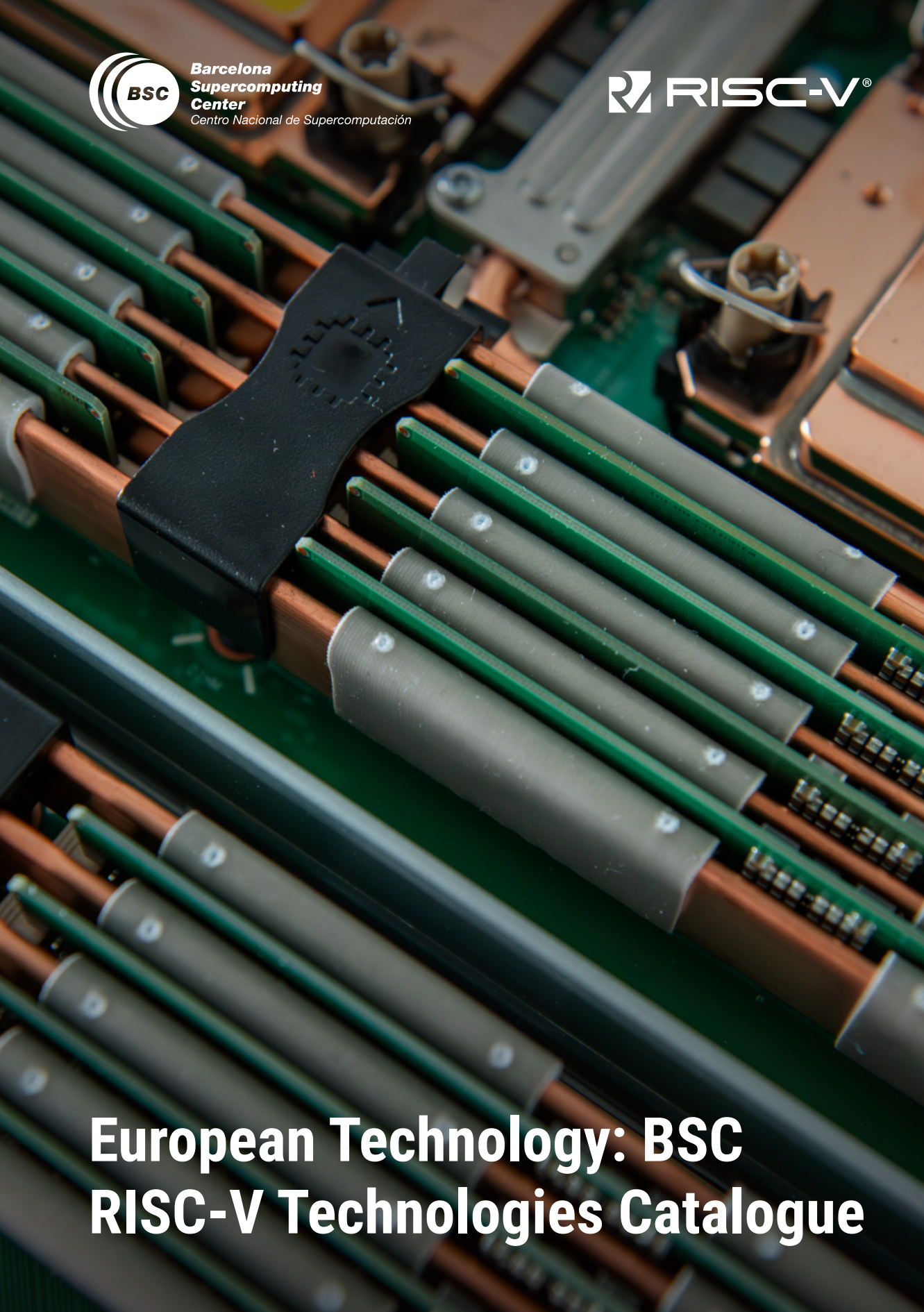

Barcelona
Supercomputing
Center
Centro Nacional de Supercomputación
RISC-V®
European Technology: BSC
RISC-V Technologies Catalogue

Driving Innovation in European Technology

BSC has strategically advanced research in RISC-V based open-source technologies in the field of HPC. It is contributing to strengthening developments in the areas of semiconductors and supercomputing by leveraging its co-design approach for contributing to the open-source software and hardware stacks. The final aim is to research novel solutions for the development of European exascale/post-exascale solution based on this technology.

As the RISC-V ecosystem continues to grow and mature, BSC is reinforcing its key role within the RISC-V European community as a Community Organization Member of RISCV International. This catalogue compiles the RISC-V based initiatives in which BSC actively contributes, and the most mature solutions designed and developed in the centre.

BSC RISC-V RELATED INITIATIVES

BSC RISC-V TECHNOLOGIES

01

BSC RISC-V **related initiatives**

Towards European open-source hardware

BARCELONA **ZETTASCALE** LAB

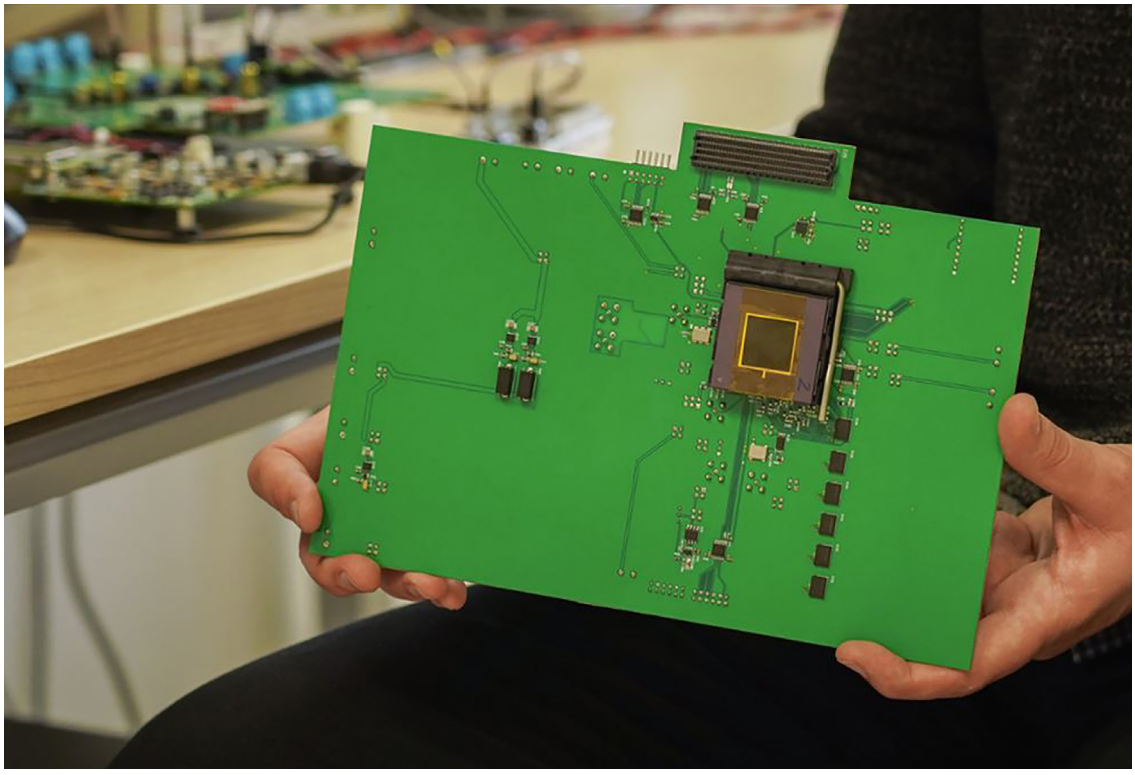
Zettascale supercomputers will be 1000 times faster than today's most powerful supercomputers. The Barcelona Zettascale Laboratory aims to develop this new generation of supercomputers.

With the aim to promote European technology, this laboratory will design microprocessors or chips with technology based on open-source RISC-V hardware.

The design of very high performance chips will be used for: supercomputers, autonomous cars and AI devices.

TECHNOLOGY

- Multicore chip design
- Mobile Manufacturers Tech
- High Performance Computing



An open source full stack ecosystem

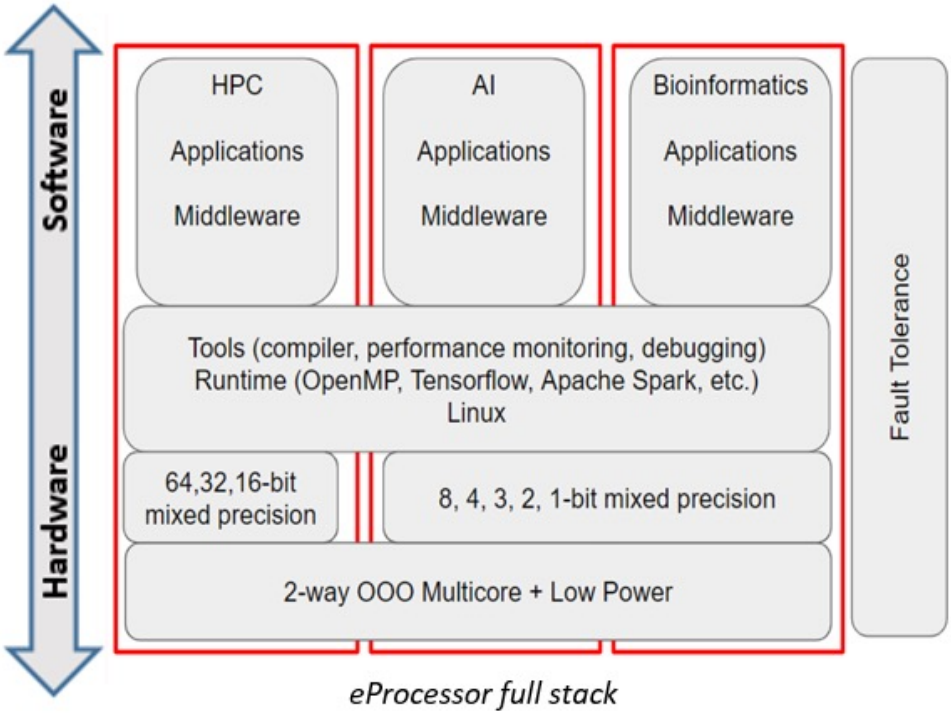
eProcessor

eProcessor presents an holistic integration of a fully open-source European full-stack ecosystem (hardware and software), featuring a novel RISC-V CPU architecture, paired with diverse and energy efficient accelerators.

The accelerators cater to traditional high-performance computing (HPC) tasks and expand into mixed precision workloads, including high-performance data analytics (HPDA), artificial intelligence (AI), machine learning (ML), deep learning (DL), and bioinformatics.

TECHNOLOGY

- Multicore chip design
- Mobile Manufacturers Tech
- Artificial inteligence
- Bioinformatics
- High Performance Computing
- Autonomous Cars



eProcessor full stack

EUPILOT: European AI/ML and HPC Accelerator System

THE EUPILOT
Pilot using Independent Local & Open Technologies

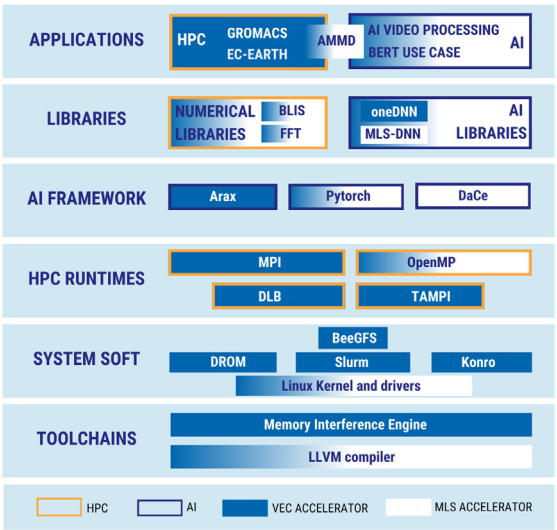
EUPILOT is an ambitious project aiming to establish a robust European computer system for high performance tasks and artificial intelligence. It's set to design, build, and validate the first EU-based accelerator platform for HPC, covering a wide spectrum of compute-intensive AI applications.

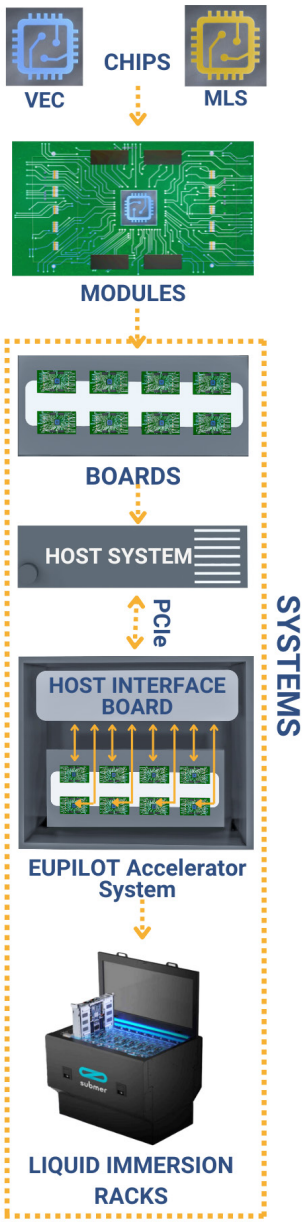
TARGET INDUSTRIES

Sector **AI, HPC, RISC-V, machine learning, semiconductors, VLSI, chips, liquid cooling, cloud computing, edge computing, genomics, molecular dynamics, datacentre computing, supercomputing, datacentre deployments, big data, data analytics, parallel computing, earth sciences, climate modeling.**

Why EUPILOT produces accelerator chips in advanced manufacturing technologies based on innovative RISC-V technologies and its associated software stack, achieving high levels of integration, efficiency, aiming to achieve a more independent technology supply chain.

Uses
- High performance computing.
- Artificial Intelligence.
- Machine Learning.
- Genomics.
- Molecular Dynamics.





European Laboratory for Open Computer Architecture (LOCA)

LOCA
European Laboratory for Open Computer Architecture

Its mission is to design and develop novel energy efficient and high performance chips based on open architectures, like RISC-V, as a response to the incremental computational, storage and power consumption demands of traditional high performance domains and beyond.

LOCA aims to provide highly optimized scientific applications in climate modeling, personalized medicine and engineering through co-design activities.

The co-design activities will go through the whole SW and HW stacks (top-down approach) starting from the characterization of real scientific HPC applications, in MareNostrum5, to the design of specific RISC-V accelerators including the toolkit to make those functional and operative.

TECHNOLOGY

- Multicore chip design
- Climate Services
- Personalized medicine
- Software Engineering
- High Performance Computing

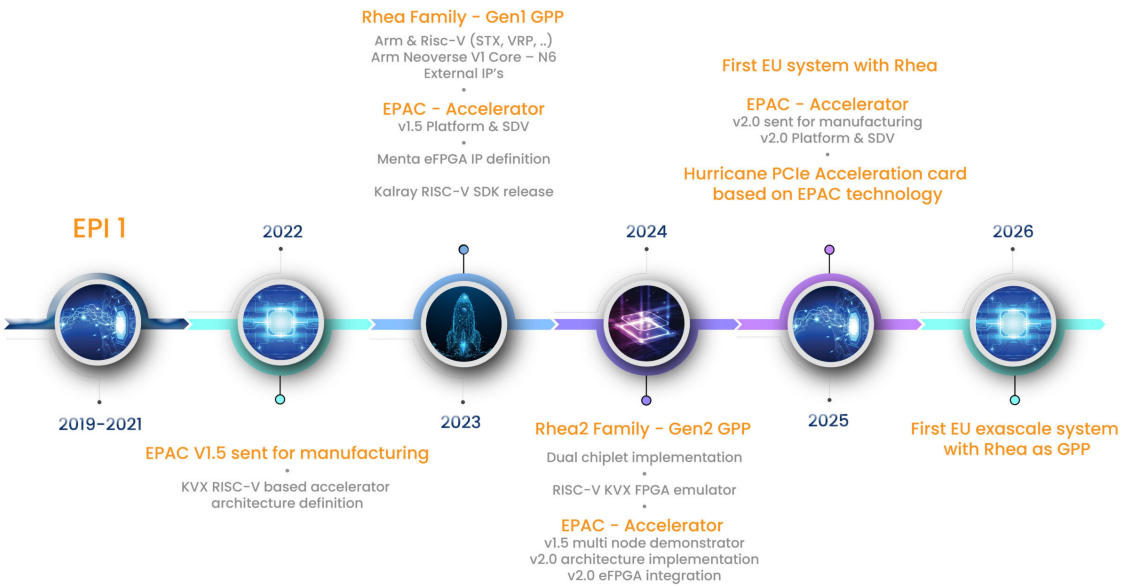
Towards European technological sovereignty

The European Processor Initiative (EPI) aims to design and build a new family of low-power processors for various applications like supercomputers and machine learning. Led by EU companies and universities, the project focuses on two main streams: developing Arm-based CPUs and RISC-V-based accelerators. BSC´s contribution includes developing a RISC-V Vector Processing Unit and software for testing and adoption in HPC.

Building a European technological sovereignty in both high-end hardware and software.

TECHNOLOGY

- Multicore chip design
- Automotive engineering
- Cloud providers
- High Performance Computing



Neuromorphic energy-efficient secure accelerators

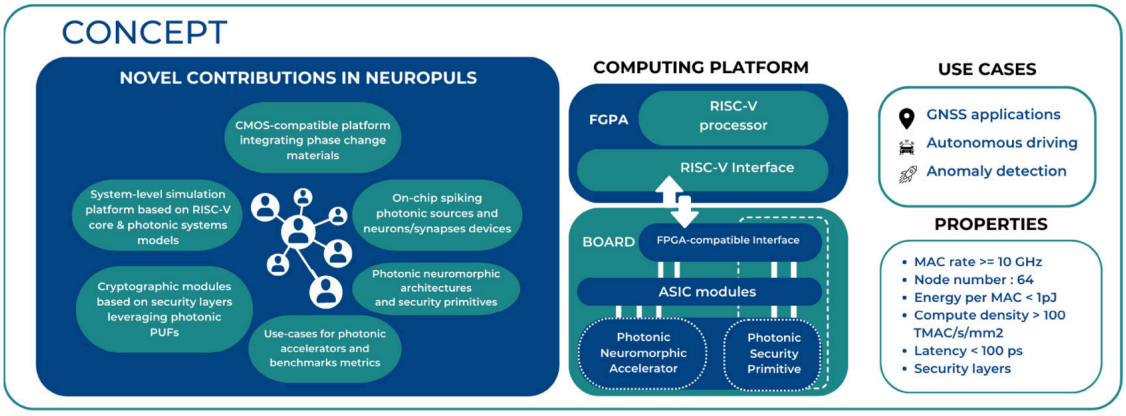
NEUROPULS

NEUROPULS aims to revolutionize the processing of massive data streams in self-driving vehicles, IoT devices, and Industry 4.0 applications. NEUROPULS aims to build low-power, secure edge computing systems by developing novel photonic computing architectures and security layers based on photonic physical unclonable functions in augmented silicon photonics platforms compatible with CMOS technology.

By developing novel technological, hardware and simulation platforms, NEUROPULS aims to create next-generation neuromorphic accelerators featuring RISC-V compliant interfaces for easier system compatibility.

TECHNOLOGY

- Multicore chip design
- Internet of Things
- Industry 4.0
- Autonomous Cars



Integrated all-European HW and Open-Source SW for Cloud Services and Applications

RISER aims for the development and validation of cloud-focused platforms, based on open standards (especially RISC-V specifications) and open source system software, packaged and configured for standards-based management and monitoring.

RISER will develop infrastructure-focused use cases in a data center setting, including: acceleration of compute-intensive processing, networked storage, and containerized execution as part of a provider-managed Infrastructure-as-a-Service environment.

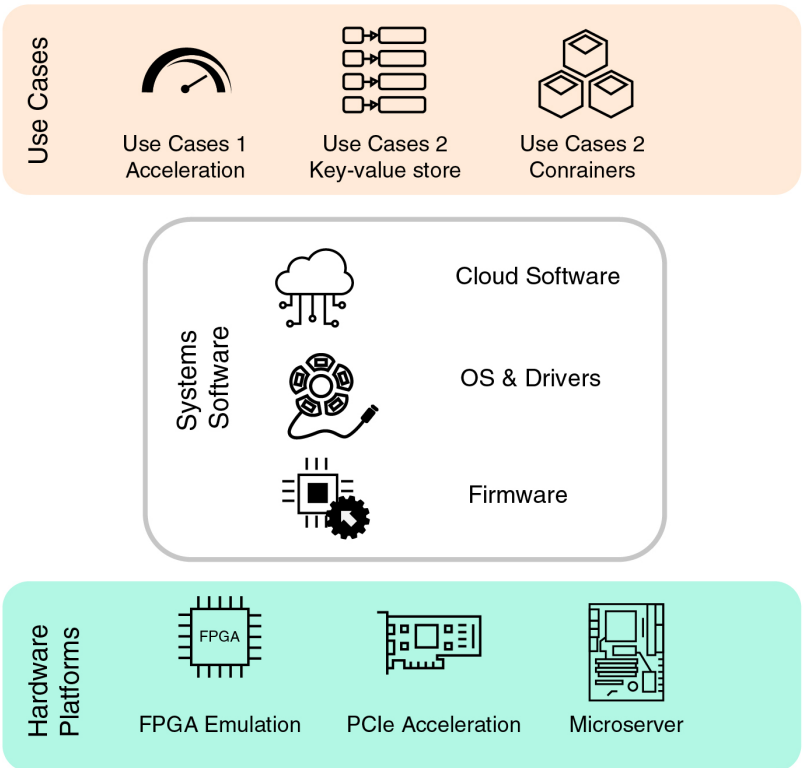
TECHNOLOGY

Cloud Computing

Cloud providers

Multicore chip design

High Performance Computing



Technology applicable to industry

SMARTY project is supported by large European industry players and well as by 10 SMEs. SMARTY's major suppliers and Original Equipment Manufacturers (OEMs) and reputable academic partners provide a great opportunity for these 10 SMEs to mature their technologies in a challenging but safe environment.

Its technology will be matured within the lifetime of the project and tested through five use cases: automotive, financial technologies, telecom and industrial settings.

SMARTY's results are applicable to different vertical sectors and can be transported to different use cases. Strong synergies with existing efforts in the area of edge computing, European processors and trustworthy AI are envisioned and planned within this initiative.

TECHNOLOGY

- Cloud software services
- Autonomous Cars
- Financial technologies
- Telecom
- Industry 4.0
- Artificial inteligence

RISC-V hardware-software stack for cloud services

Vitamin-V will deploy a complete RISC-V hardware-software stack for cloud services based on cutting-edge cloud open-source technologies for RISC-V cores.

Vitamin-V incorporates an innovative RISC-V virtual execution environment providing hardware emulation, simulation, and FPGA prototyping to enable software development, verification, and validation before actual hardware is released.

Current RISC-V hardware is energy-efficient. Vitamin-V will enable a RISC-V edge ecosystem and bring technological sovereignty to the cloud-edge continuum while reducing total cost ownership.

TECHNOLOGY

- Multicore chip design
- Cloud environment
- Big data users
- AI users
- Supply chain management

A new smart changing the whole ecosystem of automotive industry

ISOLDE will have high performance RISC-V processing systems and platforms for the vast majority of building blocks, demonstrated for key European application domains such as automotive, space and IoT with the expectation that two years after completion ISOLDE's high performance components will be used in industrial quality products.

BSC enhances, integrates and matures two components providing observability and controllability capabilities, as needed for verification, validation and safety measure realization. In particular, BSC contributes with the SafeSU statistics unit and the SafeTI traffic injector. Both are being extended with additional capabilities to monitor components and inject traffic even in a different System-on-Chip (SoC). They will be integrated as part of a Safety Island to interact with high-performance chips, and will undergo a strict validation process including appropriate safety manuals. Both BSC components, the SafeSU and SafeTI, are specifically integrated in RISC-V SoCs and will be released with open source permissive licenses to ease their adoption and the development of European safety-relevant RISC-V SoCs with high-performance capabilities.

TECHNOLOGY

Autonomous Cars

Space

Internet of Things

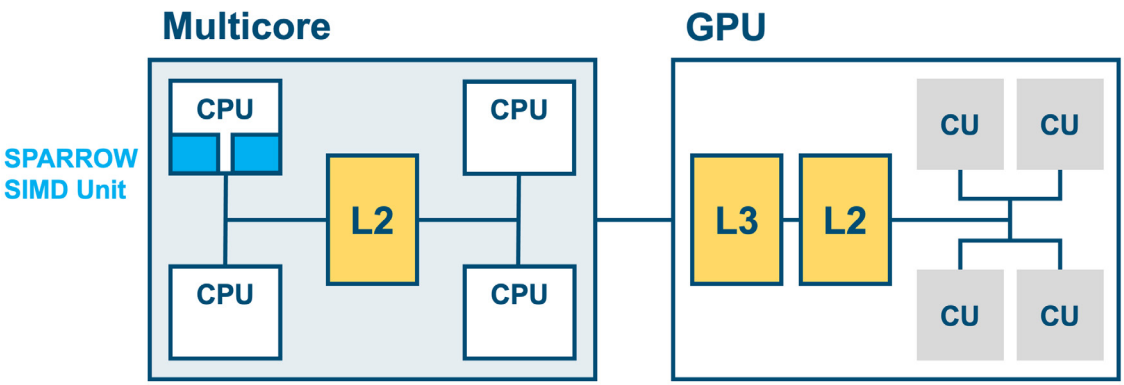
New model-based engineering methodology to design software modules

METASAT will provide a holistic and modular model-based framework to design and test software modules that target open architecture hardware, high-performance computing platforms for the space and aviation domain.

METASAT was born as a result of the need to find a solution to manage the growing complexity of new satellite designs using reliable on-board software technology.

TECHNOLOGY

- Space
- Software providers
- Multicore chip design



Perceiving a 3D world from a 3D silicon architecture

NimbleAI will design a 3D integrated sensing-processing neuromorphic chip to deliver performance and efficiency gains compared to CPU/GPUs processing frame-based video, and unlock more advanced AI and computer vision algorithms and applications.

The neuromorphic chip will mimics the efficient way our eyes and brains capture and process visual information. NimbleAI also advances towards new vision modalities not present in humans, such as insect-inspired light-field vision, for instantaneous 3D perception.

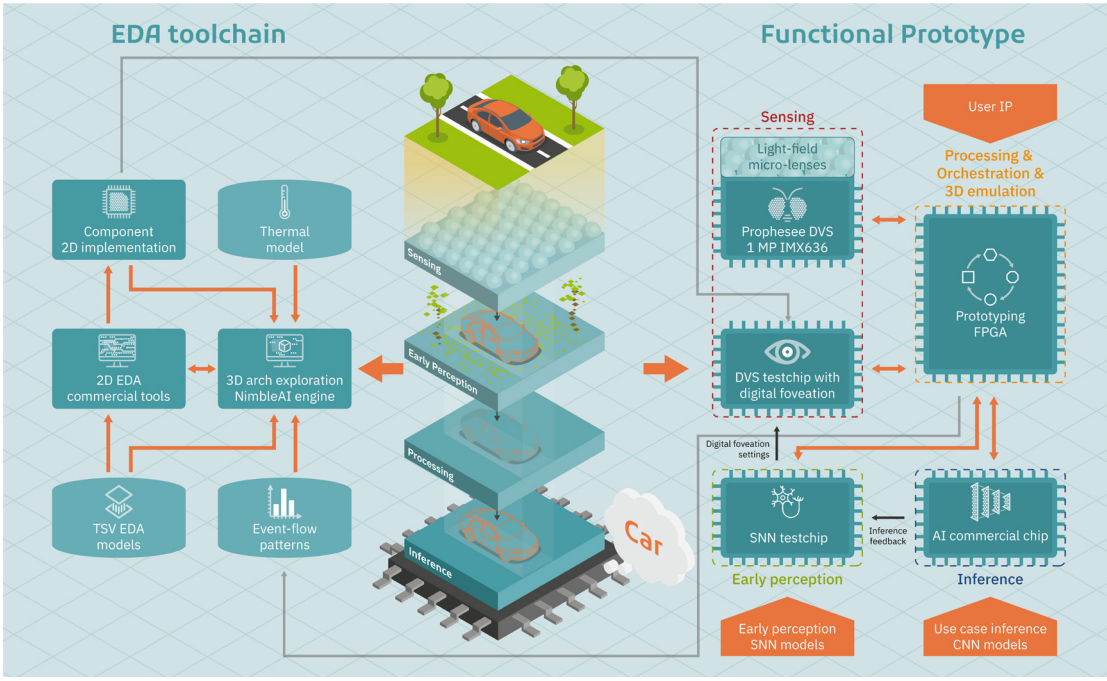
BSC is in charge of integrating and tailoring a multicore interference-aware statistics unit (SafeSU) to provide observability and controllability means for real-time performance, as well as developing and integrating a tiny controller (TinyCo) orchestrating data delivery and optimizing the processing in the NimbleAI 3D SoC.

TECHNOLOGY

Software providers

Multicore chip design

Industry 4.0



Towards fully autonomous driving

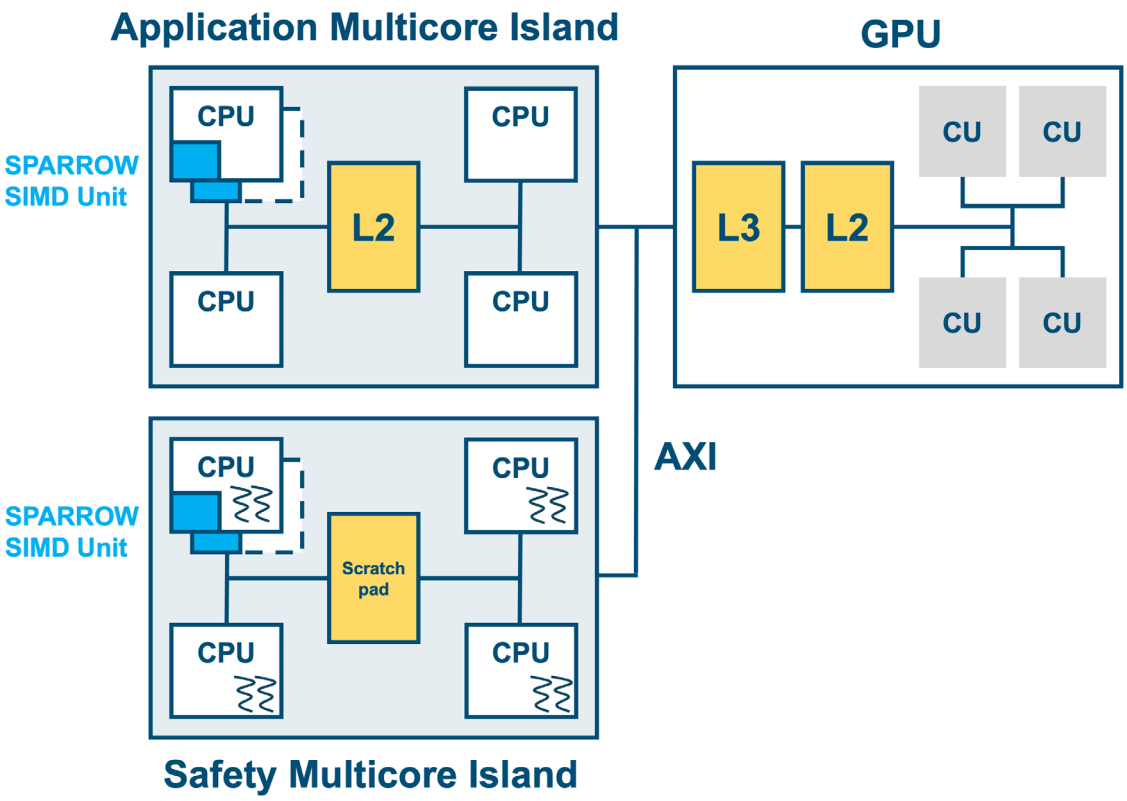
RADLER

RADLER research will be performed gradually focusing first on the implementation of a functional, hardware demonstrator of the platform on an FPGA, as well as its baseline software stack.

Once the best configuration of the hardware platform is found, the software stack will be optimized and an autonomous driving use case will be showcased. Finally, the tape out of the designed autonomous driving architecture will be performed.

TECHNOLOGY

Autonomous Cars



02

BSC RISC-V **technologies**

Lagarto Hun

Lagarto Hun is a segmented scalar processor with in-order execution, using the RISC-V open-source instruction set.

In collaboration between BSC and CIC-IPN, originally Lagarto Hun was a RV64IMA core with a 5 stages pipeline in order, supporting privileged ISA v1.11. As a first improvement, we have added support for single and double precision floating point operations, becoming Lagarto Hun into a RV64GCV + (subset RVV0.7.1) core, commonly named as RV64G for general purpose core.

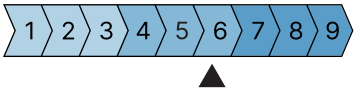
POTENTIAL APPLICATIONS

Embedded systems, education.

TYPE OF COMMERCIALISATION

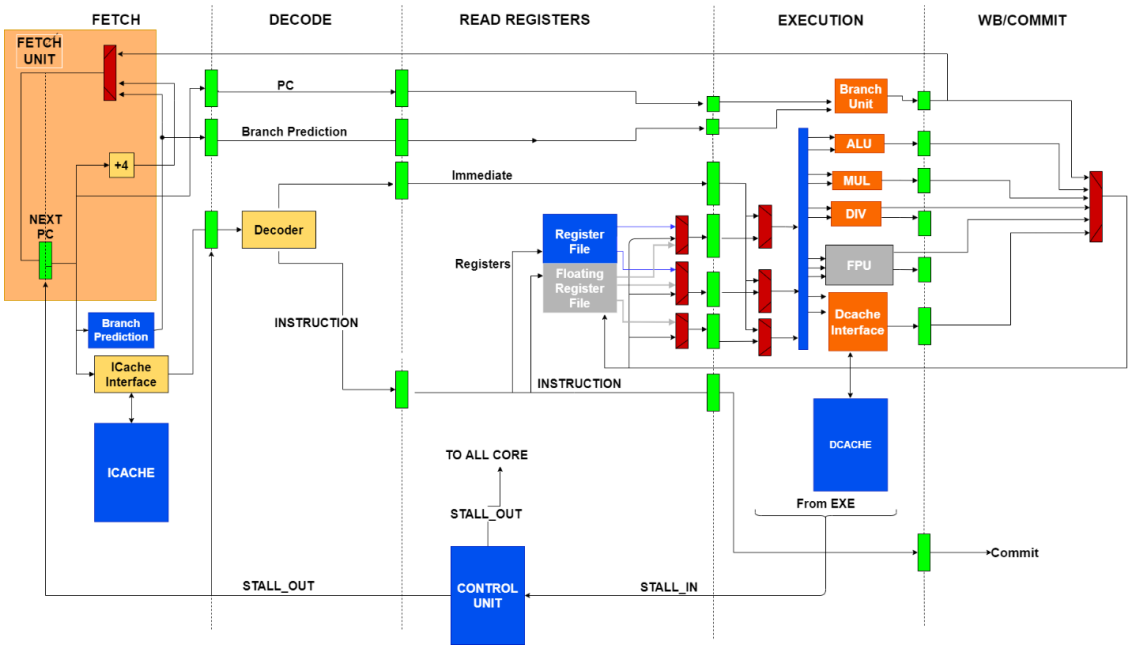
Solderpad Hardware License

TRL



MAIL

ipr@bsc.es



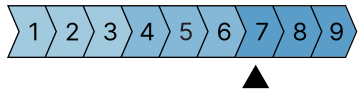
Sargantana

Sargantana constitutes the third generation of Lagarto processors, the first open-source chips developed in Spain, within the framework of the DRAC project (Designing RISC-V-based Accelerators for next generation Computers) and is one of the most academically advanced open-source chips in Europe. The new Sargantana presents better performance than its two predecessors and is the first processor in the Lagarto family to break the gigahertz barrier in working frequency.

POTENTIAL APPLICATIONS

Chip design companies can be interested in this linux-capable RISC-V core. This design is suitable for IoT and edge devices, including microcontrollers for real time applications.

TRL

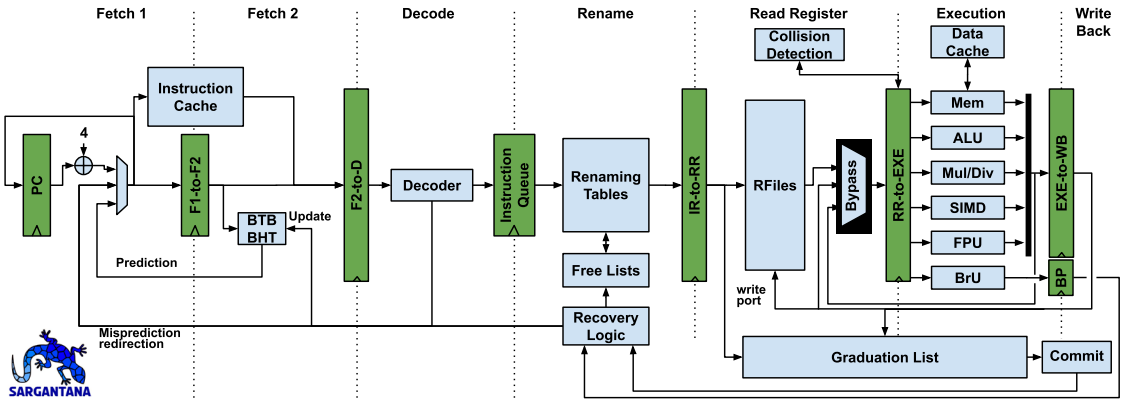


TYPE OF COMMERCIALISATION

Solderpad Hardware License (version 2.1)

URL

https://github.com/bsc-loca/sargantana



Lagarto Ka

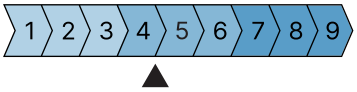
One of the main goals in processor design is achieving high performance. Various proposals from academia and industry have explored innovative ideas leveraging Moore's Law, balancing complexity and performance. Superscalar processors execute multiple instructions per clock cycle, effectively using instruction-level parallelism, dynamic scheduling, efficient memory management, and specialized accelerators.

DRAC aims to design, verify, and manufacture a high-performance processor with several accelerators in a system-on-chip (SoC). In collaboration between BSC and CIC-IPN, the Lagarto Ka processor has been proposed: a 2-way, 64-bit superscalar processor with a 12-stage out-of-order microarchitecture based on the RISC-V instruction set.

POTENTIAL APPLICATIONS

Embedded system. This design is suitable for IoT and edge devices, including microcontrollers for real time applications.

TRL

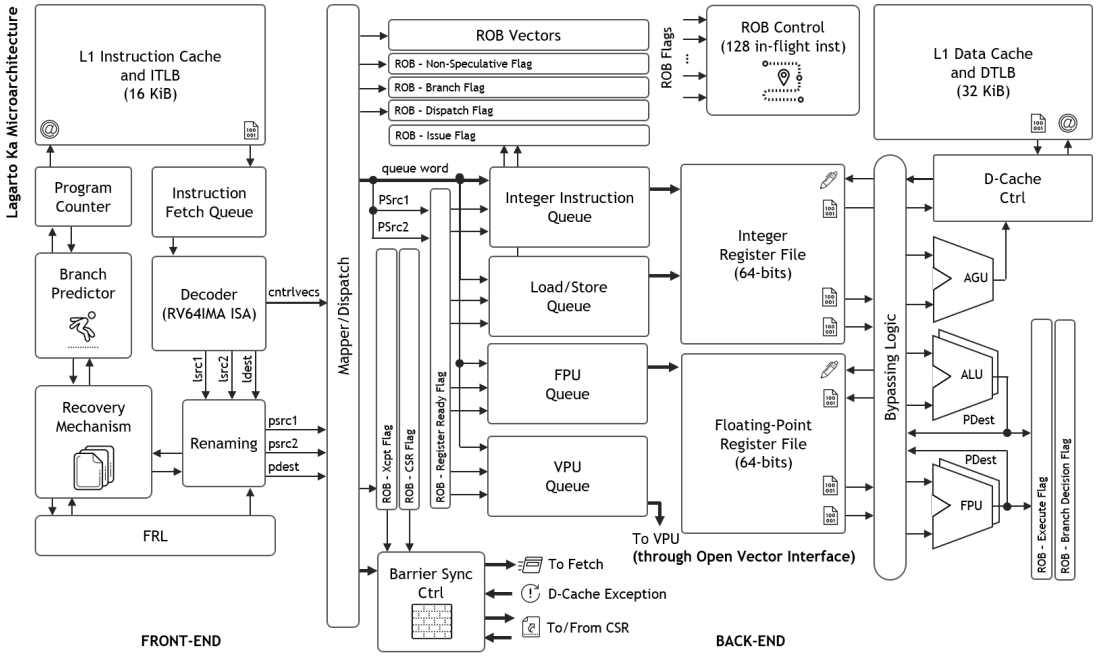


TYPE OF COMMERCIALISATION

Solderpad Hardware License (version 2.1)

MAIL

ipr@bsc.es



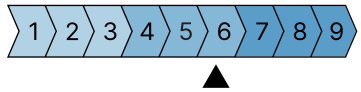
VPU

The Vector Processing Unit (VPU) is a decoupled vector accelerator with lightweight out-of-order execution capabilities. VPU targets high-performance computing (HPC) applications and is compliant with the RISC-V Vector extension 0.7.1 (RVV-0.7.1). The vector accelerator is highly parametrized which allow its implementation to instantiate a certain number of parallel execution pipelines (vector lanes), interconnected through a low-power area-efficient ring interconnect, and it can be easily connected to a scalar core through the Open Vector Interface (OVI) standard. Vitruvius version 2.0 instantiates 16 vector lanes.

POTENTIAL APPLICATIONS

High Performance Computing Applications, highly data-parallel applications.

TRL

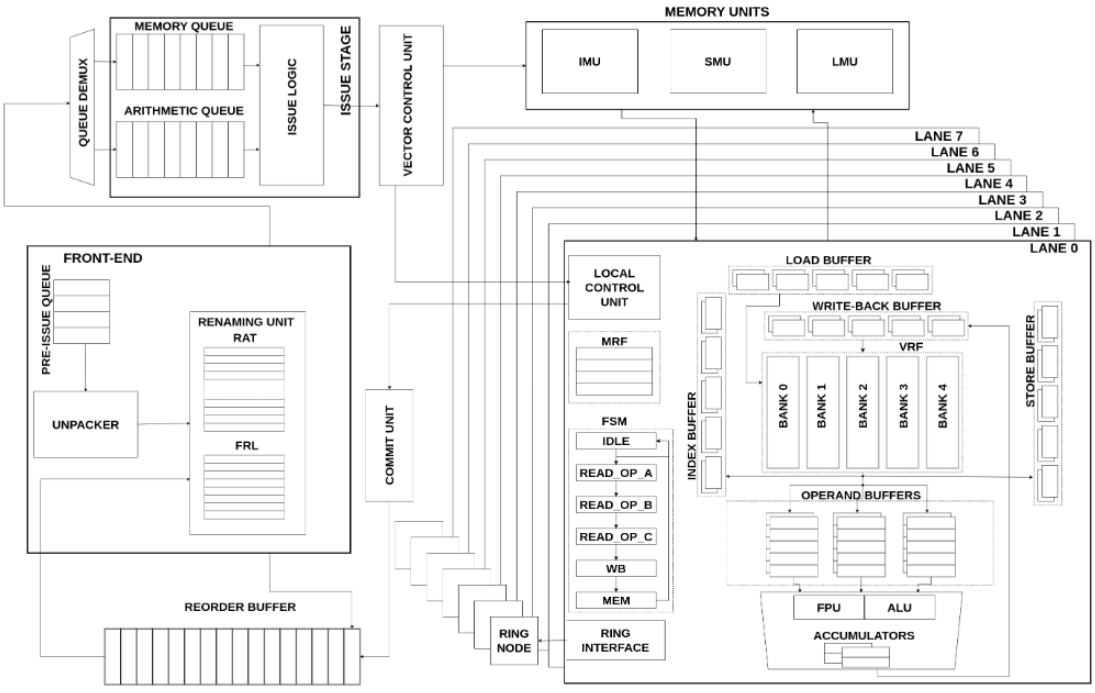


TYPE OF COMMERCIALISATION

Dual License

MAIL

ipr@bsc.es



Sauria

SAURIA is a CNN (Convolutional Neural Network) accelerator that efficiently executes heavy computations needed for neural network algorithms, such as 2D convolutions and general matrix-matrix multiplications. The accelerator is meant to be loosely coupled to a host CPU, which must manage its local memories (fetch input data and extract results) and configure its execution through a memory-mapped interface. Once the host has prepared and started the execution, SAURIA will perform the convolution independently, and raise an interrupt upon full completion.

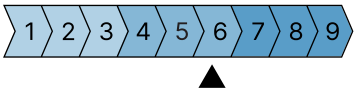
POTENTIAL APPLICATIONS

Devices that target machine learning applications can use this architecture to speed-up computation and improve efficiency. While the hardware specifications may not be superior to similar products in the market, we integrate it with a RISC-V core and publish our work as open source, while most existing products are closed-source and work with closed ISAs.

TYPE OF COMMERCIALISATION

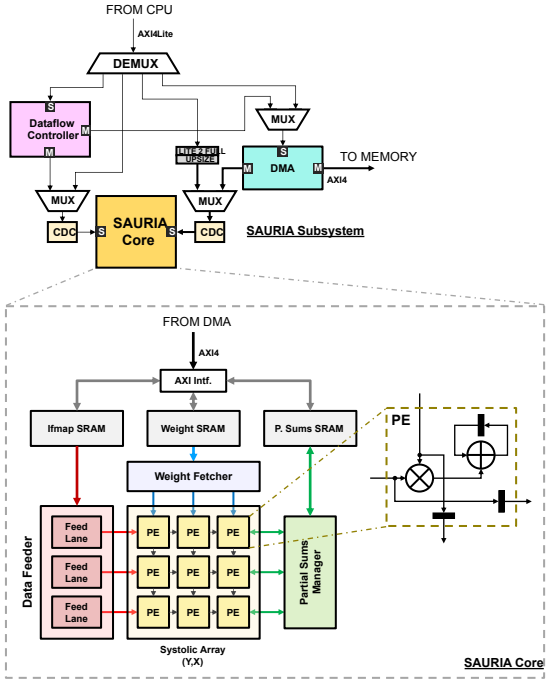
Solderpad Hardware License (version 2.1)

TRL



URL

https://github.com/bsc-loca/sauria



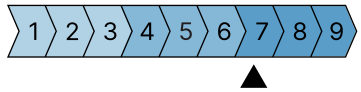
ProNoc

ProNoC presents an FPGA-optimized Network-On-Chip RTL code with ASIC-based NoC functionalities. ProNoC offers a fully parametrizable design written in SystemVerilog. The NoC is configurable with many state-of-the-art features such as virtual channels, virtual networks, hard-built-in QoS, multicast, multihop bypass, different routing algorithms, and network typologies.

POTENTIAL APPLICATIONS

The ProNoC RTL code can be used as a crosspoint IP core in any multicore system while offering a low-cost and low-communication latency interconnection network.

TRL

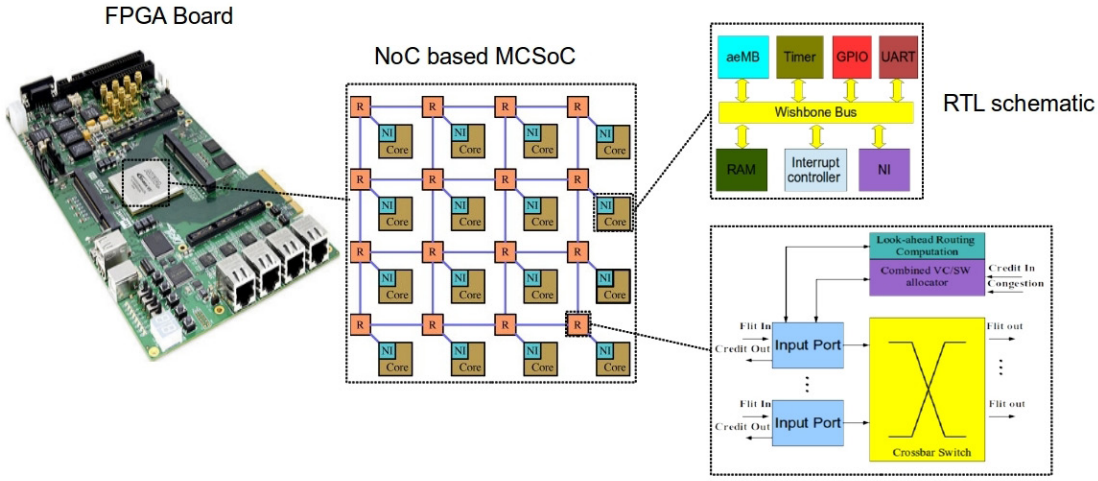


TYPE OF COMMERCIALISATION

Solderpad Hardware License (version 2.1)

URL

https://github.com/bsc-loca/ProNoC



Extensions to OpenPiton

OpenPiton is an open-source scalable framework for supporting different cores interconnected through a NoC. It integrates the OpenPiton design in new FPGA HW platform: Alveo U280. The addition will help other designers to use OpenPiton in a different HW platforms further than the ones provided by the OpenPiton Framework by default.

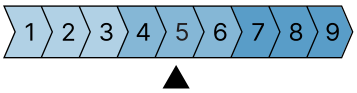
POTENTIAL APPLICATIONS

HPC for multicore system or accelerators.

TYPE OF COMMERCIALISATION

Apache License (version 2.0)

TRL



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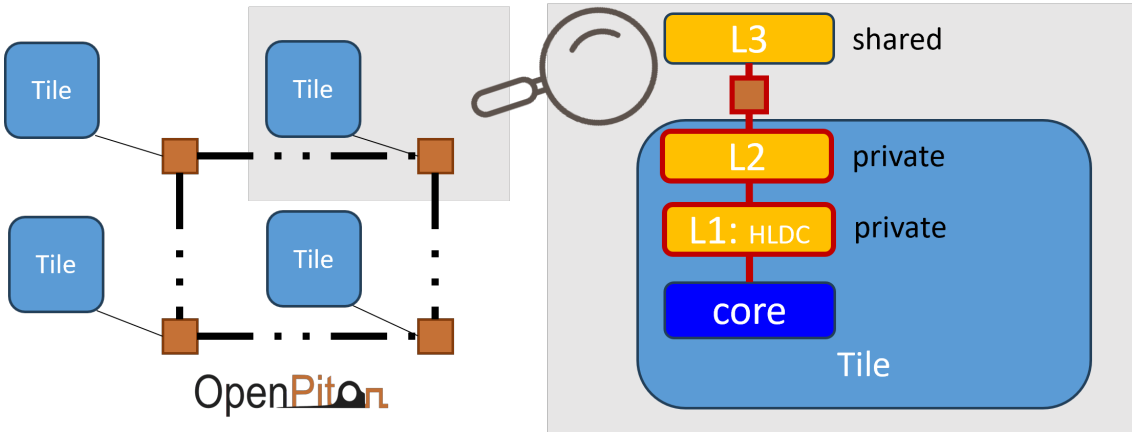


Classic McEliece Accelerator

This technology is a hardware/software co-design acceleration. The software part is an accelerated version of the purely software implementation of the post-quantum security named Classic McEliece and is being executed at a CPU.

The hardware part, which is High-Level-Synthesis based, is being mapped on an FPGA (Field Programmable Gate Array) device. The current hardware module implements the Classic McEliece's Key Encapsulation Mechanism algorithms of encryption and decryption. Its purpose is to accelerate the execution of the aforementioned algorithms in the context of a SoC integration.

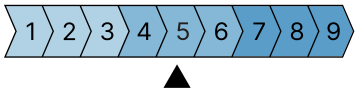
POTENTIAL APPLICATIONS

Possible commercial applications could include the execution of this technology on a heterogeneous System on Chip comprising a CPU and an FPGA device. This SoC could be part of any product that requires post-quantum security protection. Also, the hardware accelerator can be used as a loosely coupled accelerator to the CPU pipeline in order to speed-up the encryption and decryption algorithms of the Classic McEliece Post-Quantum Key Encapsulation Mechanism.

TYPE OF COMMERCIALISATION

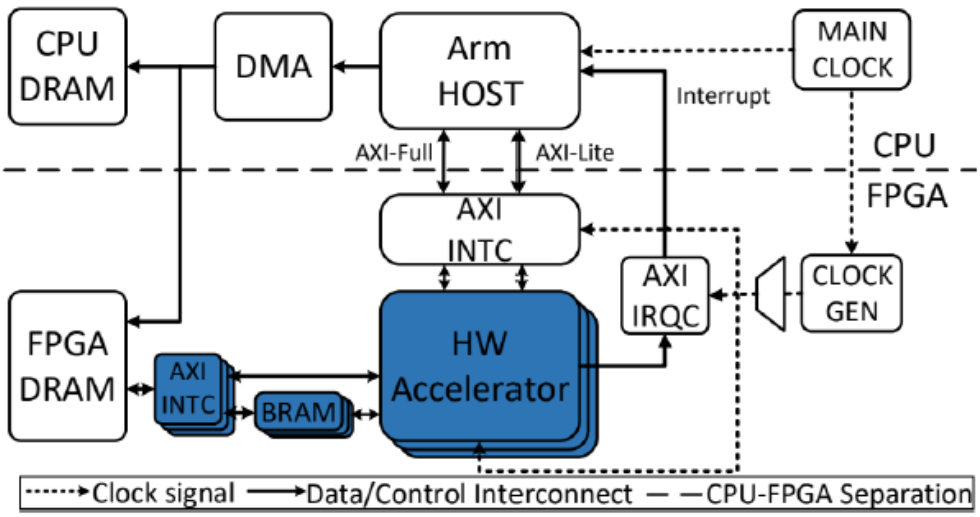
BSD License (version 3)

TRL



URL

https://github.com/beatsnbytes/classic_mceliece



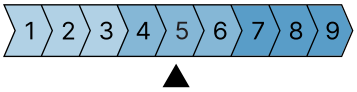
RISC-V SoC Integration of PQC Accelerator for CRYSTALS-Kyber KEM and CRYSTALS-Dilithium Ds Schemes on FPGA

This technology implements a Post-Quantum Cryptographic (PQC) accelerator to integrate it inside a System On Chip (SoC) for FPGA. The module, implemented in a High-Level Synthesis (HLS) approach, accelerates two PQC schemes, the CRYSTALS-Kyber and the CRYSTALS-Dilithium. On the one hand, CRYSTALS-Kyber is a key-encapsulation mechanism (KEM) belonging to asymmetric cryptography. Whose security is based on the difficulty of solving the learning-with-errors (LWE) problem over module lattices. On the other hand, CRYSTALS-DIlithium is a Digital Signature Scheme (DSS). It is strongly secure under chosen message attacks based on the hardness of lattice problems over module lattices. The security notion means that an adversary with access to a signing oracle cannot produce a signature of a message whose signature he hasn't yet seen nor produce a different signature of a message he already saw signed. Then, both schemes (Kyber and Dilithium) are the candidate algorithms to be standardized by the NIST post-quantum cryptography project.

POTENTIAL APPLICATIONS

The proposed hardware can be applied to improve the computation of Post-Quantum Cryptographic Key Encapsulation Mechanisms and Digital Signature Schemes algorithms.

TRL



TYPE OF COMMERCIALISATION

Solderpad Hardware (version 0.51)

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ipr@bsc.es

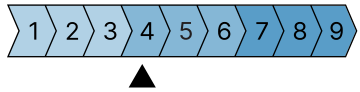
Bison

The proposed technology is a set of instructions capable of accelerating dense linear algebra operations composed of narrow-integer data types. It relies on a mathematical technique, called Binary Segmentation. This technique enables two main advantages, data compression in memory for data types that are smaller than the computer bit width, and arithmetic complexity reductions of a set of dense linear algebra arithmetic vector operations, such as additions/subtractions, reductions, inner-products, linear convolutions.

POTENTIAL APPLICATIONS

The proposed hardware can be applied to improve the computation of several application fields, such as Deep Learning, String Matching, Graph Processing, Cryptography.

TRL

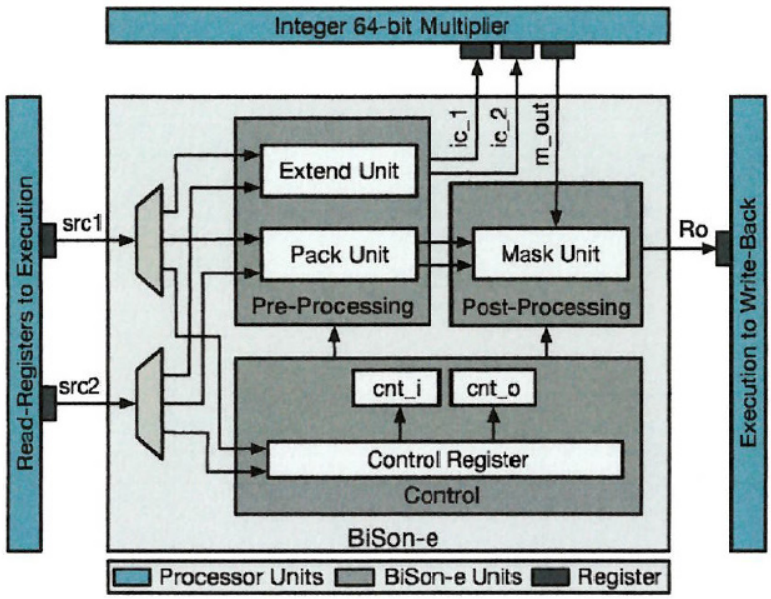


TYPE OF COMMERCIALISATION

Patent

URL

https://www.bsc.es/es/tech-transfer/technology-offer/patents-portfolio/method-the-computation-narrow-bit-width-linear



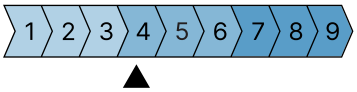
Vaquero

VAQUERO is a Vector Acceleration for Query Processing that improves the efficiency of vector architectures for DBMS operations such as data aggregation and hash joins featuring lookup tables.

POTENTIAL APPLICATIONS

By including VAQUERO hardware in a commercial CPU, the execution time need to process a query in a Database Management System gets reduced by 3x – 6x.

TRL



TYPE OF COMMERCIALISATION

Patent

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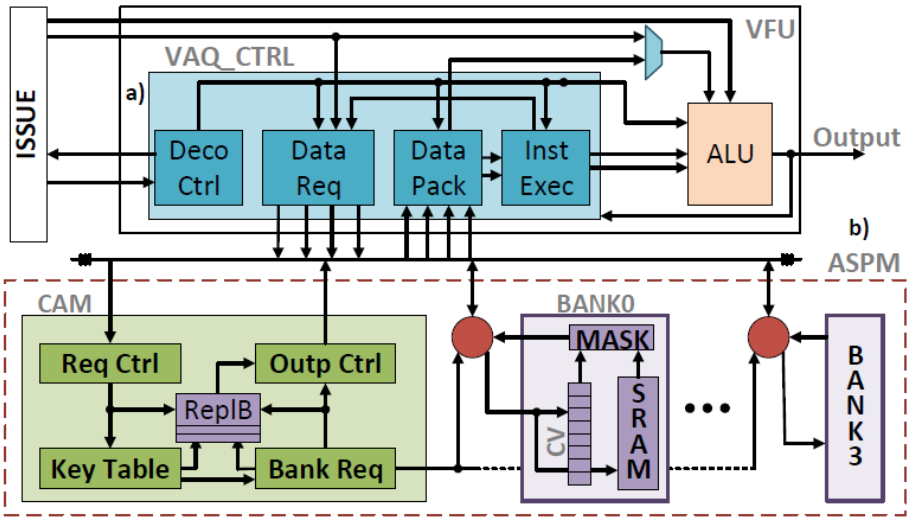


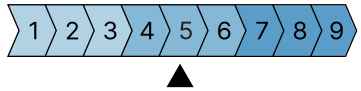
SafeSU

The Safe Statistics Unit is an RTL digital IP (Intellectual Property) of and advanced statistical unit including controllability and observability channels to enforce and validate multicore interference, and diagnose the root cause of overflows.

POTENTIAL APPLICATIONS

It could be licensed for use on commercial applications in the future. A free to use model with paid commercial support may be feasible in the future.

TRL

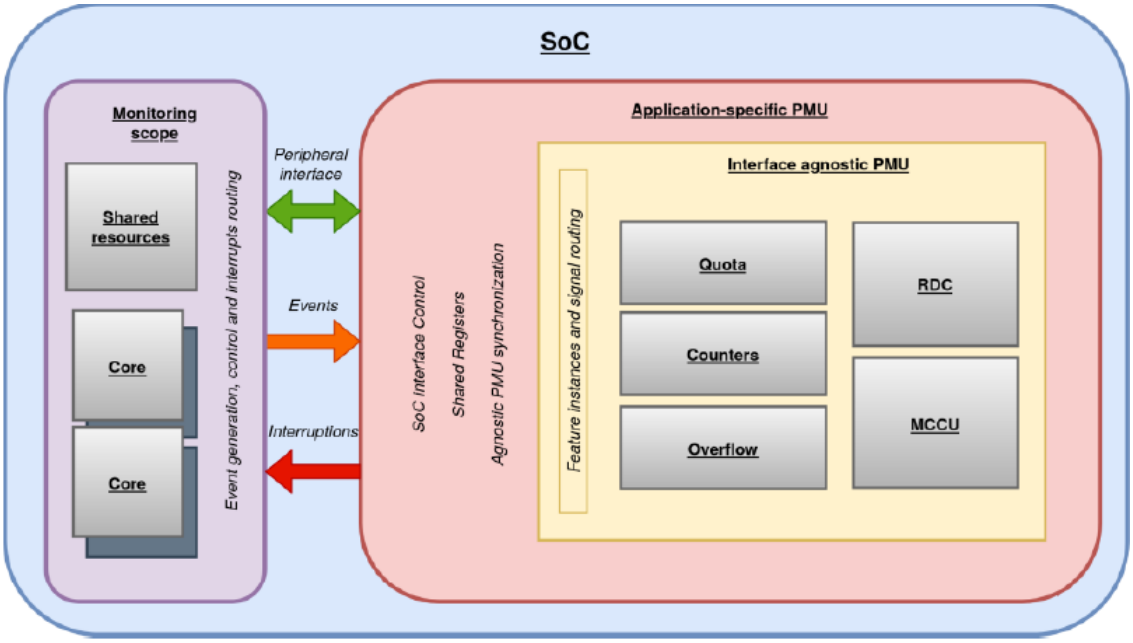


TYPE OF COMMERCIALISATION

MIT License

URL

https://github.com/bsc-loca/SafeSU



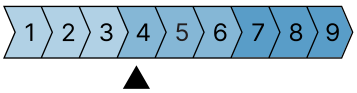
SafeTI

The Safe Traffic Injector (SafeTI) is an RTL digital IP (Intellectual Property) of an advanced traffic injector unit which allows injecting programmable traffic in AMBA AHB interconnects with high flexibility and degree of control, thus easing achieving high coverage in terms of traffic scenarios tested and mitigating the uncertainty due to the difficulties to relate software tests with actual traffic scenarios tested.

POTENTIAL APPLICATIONS

It has a modular architecture that eases integration into a variety of multiprocessor platforms.

TRL

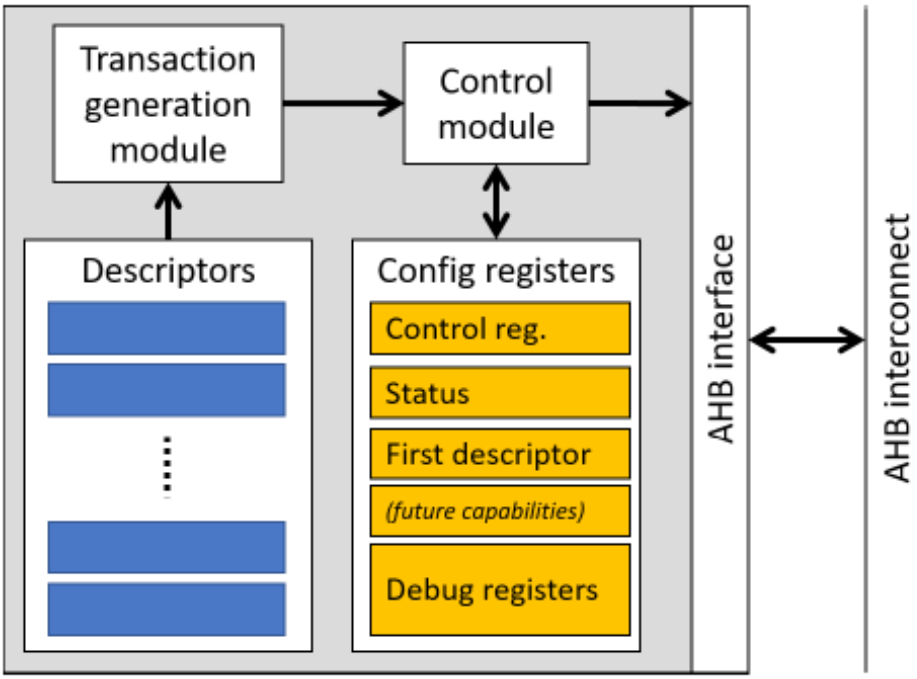


TYPE OF COMMERCIALISATION

MIT License

URL

https://github.com/bsc-loca/Safeti



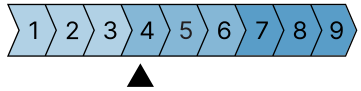
SafeDE

SafeDE is an RTL digital IP (Intellectual Property) of a hardware monitor that allows coupling two independent cores to operate in lockstep mode. Lockstepped execution is needed to avoid Common Cause Failures due to Common Cause faults. Current lockstep schemes have a significant penalty in terms of performance (the user sees two coupled cores just like one). SafeDE overcomes this limitation by offering the flexibility to change between lockstepped and normal execution depending on the criticality of the tasks. SafeDE is attached to the AMBA APB interface, so every system including an APB interface can easily integrate SafeDE. SafeDE is controlled by means of three internal registers that are modified through standard load and store operations.

POTENTIAL APPLICATIONS

For use in automotive, avionics, spacial, robotics, railways or healthcare areas.

TRL

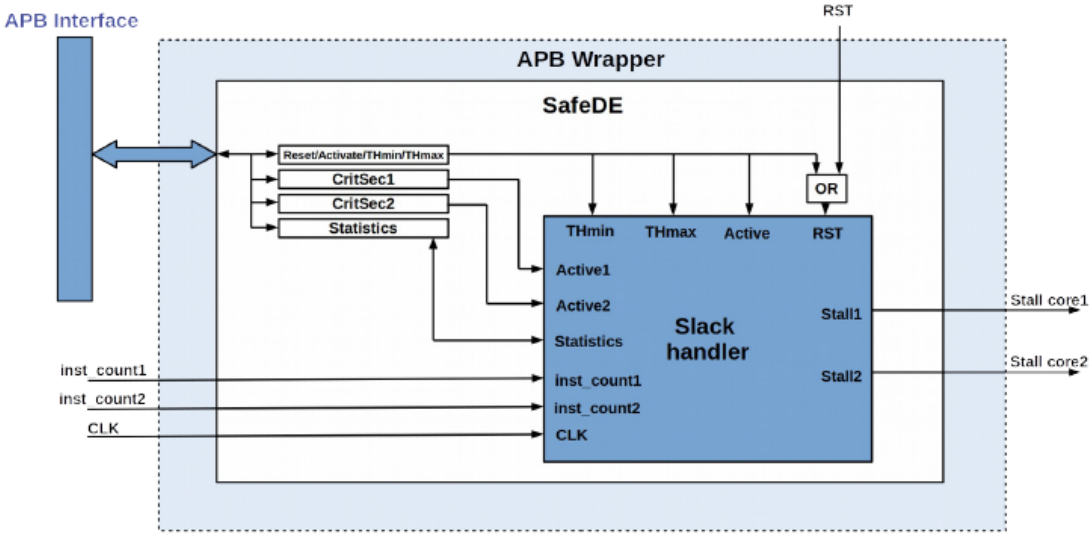


TYPE OF COMMERCIALISATION

MIT License

URL

https://github.com/bsc-loca/SafeDE



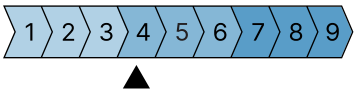
SafeDM

SafeDM is a hardware Diversity Monitor that quantifies the diversity of each redundant processor to guarantee that CCF will not go unnoticed, and without needing to deploy lockstepped cores. SafeDM computes data and instruction diversity separately, using different techniques appropriate for each case.

POTENTIAL APPLICATIONS

Effective hardware solution to quantify diversity in cores performing redundant execution. For use in automotive, avionics, spacial, robotics, railways or healthcare areas.

TRL

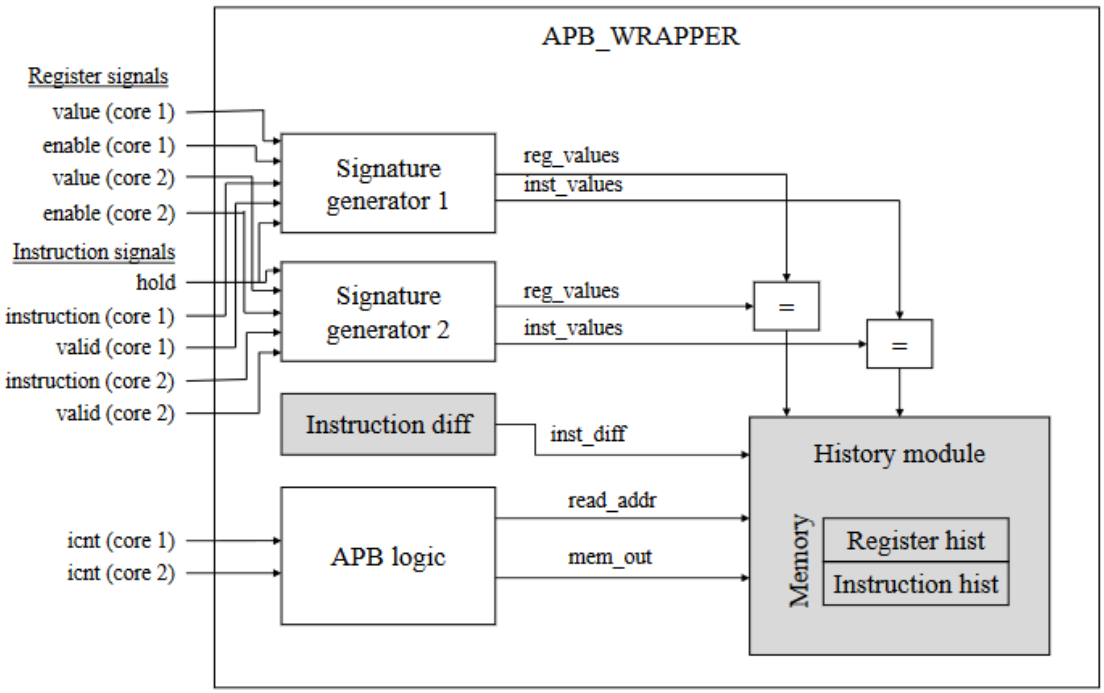


TYPE OF COMMERCIALISATION

MIT

URL

https://github.com/bsc-loca/SafeDM



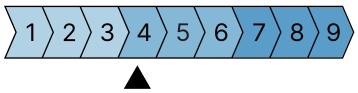
SafeLS

SafeLS (Safe Lockstep): The Safe Lockstep (SafeLS for short) unit is a RISC-V open-source lockstep core based on Frontgrade Gaisler AB's NOEL-V core for the space domain, as well as its integration in the SELENE SoC that provides a complete microcontroller synthesizable on FPGA successfully assessed against space, automotive, and railway safety-critical applications in the past.

POTENTIAL APPLICATIONS

For use in automotive, avionics, spacial, robotics, railways or healthcare areas.

TRL

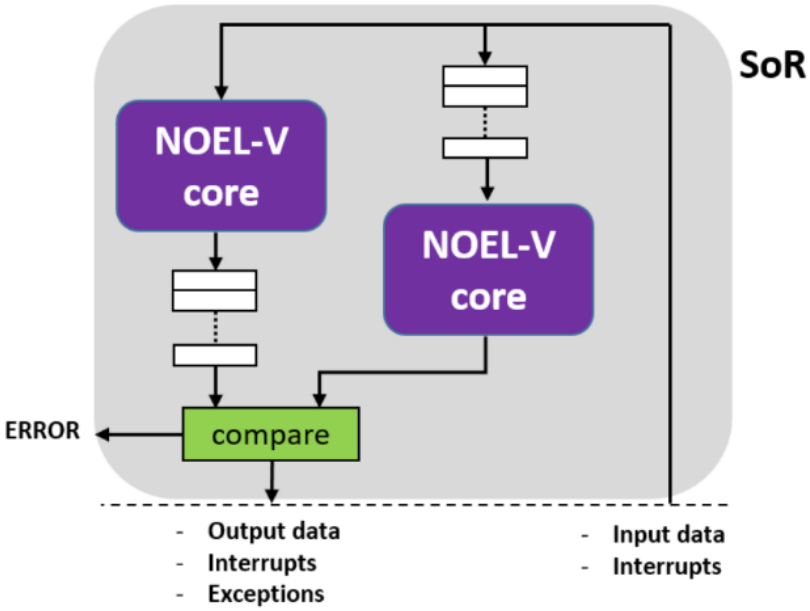


TYPE OF COMMERCIALISATION

GPL version 3

URL

https://github.com/bsc-loca/Safels



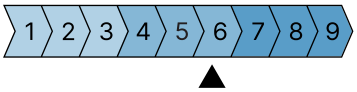
LLVM Compiler Optimizations for RVV

This is a compiler that implements the EPI requirements when it comes to vectorization for RISC-V Vector Extension. This compiler includes an implementation of the EPI-specific intrinsics and the vectorizer for the RISC-V Vector Extension. This compiler enables vectorization of applications using the RISC-V Vector Extension either using the mentioned intrinsics or the automatic vectorization mechanism. The vectorization mechanism can be triggered automatically or explicitly requested via pragma annotations such as #pragma clang loop or #pragma omp simd.

POTENTIAL APPLICATIONS

Development of applications for EPAC so that they can take advantage of the system's functionalities. In particular, the compiler allows exploiting the vector capabilities of EPAC's VEC accelerator.

TRL



TYPE OF COMMERCIALISATION

Apache License (version 2.0)

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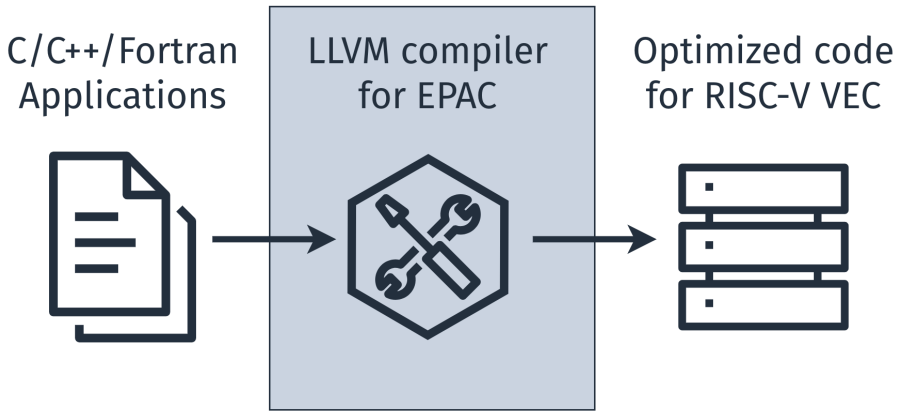

Vehave

Vehave is a native functional emulator. It was born out of necessity of being able to functionally test the generated vector code on top of a RISC-V Linux system.

POTENTIAL APPLICATIONS

Useful to obtain trace-level information for analysis and modelling.

TYPE OF COMMERCIALISATION

Apache License (version 2.0)

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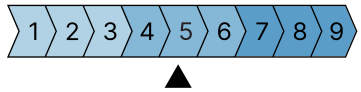

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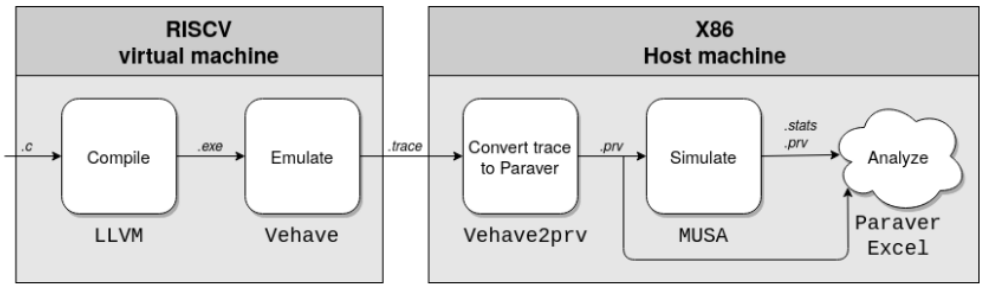


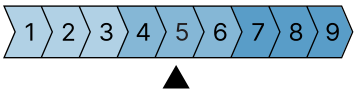
GMX: Instruction Set Extensions for Genome Sequence Alignment

GMX, a set of ISA extensions that enable efficient sequence alignment computations based on dynamic programming (DP). GMX extensions provide the basic building-block operations to perform fast tile-wise computations of the DP matrix, reducing the memory footprint and allowing easy integration into widely used algorithms and tools.

POTENTIAL APPLICATIONS

The proposed hardware can be applied to improve the computation of several genome sequence alignment applications with minimal hardware cost.

TRL



TYPE OF COMMERCIALISATION

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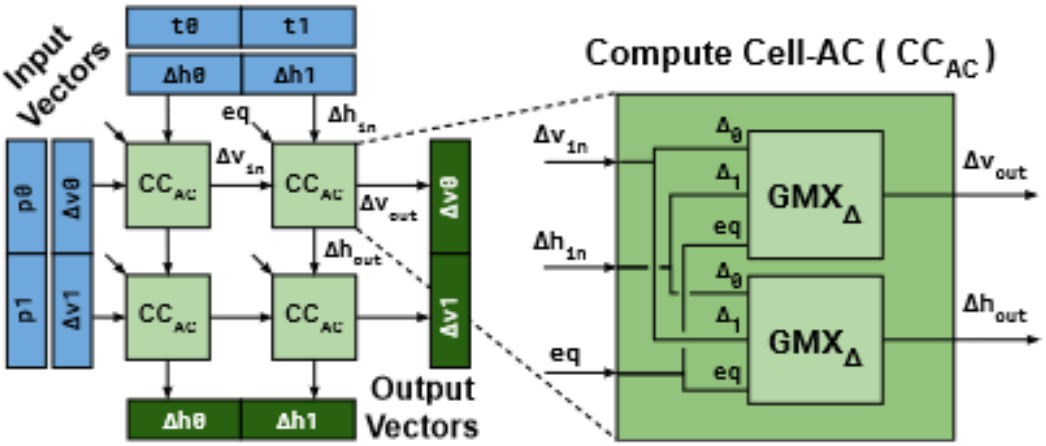

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