IBM-BSC - Malleable Vector Processor Microarchitecture

Malleable Vector Processor Microarchitecture

This SoW supports the research effort towards the malleable vector processor microarchitecture. In particular, this SoW is working in four directions:

1. it is developing a new malleable register file organization for vector processors;
2. it is carrying out a software-hardware co-design study to optimize the performance of sparse operations on vector processors;
3. it is exploring how to leverage block based floating point representations by compressing the mantissa values; and
4. it is developing RTL design, verification and physical design of the selected ideas developed across the whole project.

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