

Vector Processing Unit (VPU)

Vitruvius targets high-performance computing (HPC) applications and is compliant with the RISC-V Vector extension 1.0 (RVV-1.0). The vector accelerator is highly parametrized which allow its implementation to instantiate a certain number of parallel execution pipelines (vector lanes), interconnected through a low-power area-efficient interconnect. The number of parallel lanes, as well as the maximum hardware-supported vector length, is an implementation parameter which can be freely set to target different application domains.

It may be used for High Performance Computing Applications as well as highly data-parallel applications.

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