Multi-core microbenchmark technology (m?BT)

BSC's microbenchmark technology

Multi-core processors are becoming the baseline computing solution in critical embedded systems. While multi-cores allow high software integration levels, hence reducing hardware procurement and SWaP (Space, Weight and Power) costs, their use challenge current practices in timing analysis.

When planning to use multi-cores, critical real-time system practitioners face the following challenges:

BSC's m?BT speeds up multi-core adoption. m?BT consists of a set of specialized user-level benchmarks that put high load on multi-cores' shared resources. By running BSC's microbenchmarks against your reference application under analysis, you will get an accurate measure of the impact that resource contention may have on your application's timing behaviour.

m?BT comprises a validation loop that works with Performance Monitoring Counters (PMCs) to provide evidence that the microbenchmarks achieve their intended goal in stressing different processor resources.

m?BT can be tailored for a wide set of multi-core processors. BSC also offers its 10+ years of experience in multi-core contention analysis to help you to achieve the requirements of certification authorities for the use of multi-cores. For avionics, BSC provides its experience to accomplish CAST32A recommendations in identifying contention (interference) channels, establishing hardware setups that limit contention and providing evidence of the degree of isolation.

BSC's microbenchmark technology can be used not only for performance but also for energy/power analysis. Architectures analysed using BSC's m?BT include: the IBM POWERX family of processors; ORACLE Niagara T2; Cobham Gaisler's NGMP; and the AURIX TX277x family.

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