# Lagarto KA

DRAC aims to design, verify, and manufacture a high-performance processor with several accelerators in a system-on-chip (SoC). In collaboration between BSC and CIC-IPN, the Lagarto Ka processor has been proposed: a 2-way, 64-bit superscalar processor with a 12-stage out-of-order microarchitecture based on the RISC-V instruction set.

It may be used for embeddded systems. This design is suitable for IoT and edge devices, including microcontrollers for real time applications.

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