SORS: A View of the Future of Memory Technologies and Systems

Objectives

Abstract: This will be a highly interactive presentation on the future of memory technology and the implications on the future of memory systems provided by one who has been at the heart of the past 27 years of advancements in memory technology and memory and systems architecture. In this talk we will explore the future of DDR memories, 3D-stacked and 3D natural memories, emerging memory technologies, future memory hierarchy and the practical implications, practical possibilities of more than memory functions in memory or in memory stacks. Come armed with your questions.

Short bio: As Senior Director of Architecture Development in Micron's NetCom group, Thomas Pawlowski is responsible for Micron memory product definition for networking andcommunications applications. During his tenure at Micron, Tom has created or co-createdthe following devices: Reduced Latency DR AM-II, Pipelined Burst Synchronous SRAM,Zero Bus Turnaround SRAM, Double Data Rate SRAM and Quad Data Rate SRAM.Tom holds over 80 U.S. and international patents, with more pending. Prior to joining Micron in 1992, Tom's spent eight years at Allied Signal Aerospace. Heholds a bachelor of applied science degree in electrical engineering from the Universityof Waterloo, Ontario, Canada.

Speakers

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