SORS: GPU@SAT: Empowering Edge Computing for AI Onboard Satellites

Abstract

In satellites, real-time processing often generates data that exceeds onboard computational capabilities. Traditionally, this data is transmitted to Earth for analysis. However, edge computing has shifted processing directly onboard satellites, reducing latency, optimizing bandwidth, improving reliability, and lowering costs. A major focus in this field is accelerating Machine Learning (ML) and Deep Learning (DL) algorithms onboard, enabling low-latency data filtering and enhanced mission performance. These algorithms, however, are computationally demanding and require dedicated accelerators that balance high performance with strict constraints on size, power, and resilience to harsh space conditions.

This research introduces GPU@SAT: a 32-bit soft-Graphic Processing Unit (GPU) core implemented in VHDL and designed for Field Programmable Gate Arrays (FPGAs). GPU@SAT is intended as an accelerator for ML/DL algorithms onboard satellites. Its parallel structure and compatibility with OpenCL make it efficient for accelerating neural network computations such as matrix multiplications and convolutions. Additionally, its FPGA implementation facilitates radiation resistance, flexibility, and scalability. To date, GPU@SAT has been implemented on Xilinx Zynq UltraScale+ MPSoC evaluation boards at frequencies up to 250 MHz. It also has been integrated in a larger development environment, the GPU@SAT DevKit, which simplifies the programming and testing of applications via a client/server approach that abstracts the complexities of the accelerator. Preliminary results demonstrate its potential, offering an innovative solution to enhance computational capabilities onboard satellites.

Short Bio

Giovanni Todaro is a third year Ph.D. student in Information Engineering at University of Pisa. During his academic years, he showed particular interest in the world of digital design, specializing in embedded system design for FPGAs. Nowadays, his research focuses on the design and improvement of innovative programmable architectures with a general-purpose structure that can support and then improve the execution of Artificial Intelligence (AI) algorithms for space applications. With his research, he intends to make computing onboard satellites more efficient to reduce their energy consumption and increase the overall duration of space missions. His doctoral fellowship is co-funded by the company IngeniArs S.r.l. He will be visiting BSC for a research collaboration with the Programming Models Team, partially funded by the Severo Ochoa project, until July 2025.

Speakers

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