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Abstract

This talk will describe two adjacent projects from our team. The first is the application of high performance computing (HPC) techniques to enable scalable RTL simulation for 10B transistor-scale designs. Our tool, Metro-MPI, exploits the natural boundaries present in chip designs (such as latency-insensitive interfaces) to partition RTL simulations and HPC techniques to extract parallelism. Our implementation of Metro-MPI in OpenPiton+Ariane delivers 2.7 MIPS of RTL simulation throughput for the first time on a design with more than 10 billion transistors and 1,024 Linux-capable cores, simulated on 1000+ physical cores.

The second project introduces the problem of hardware decompileation, analysing a low-level artifact (a netlist) in order to recover higher-level programming abstractions, and using those abstractions to generate code written in an HDL. To start attacking this problem, we focus on hardware loop rerolling, identifying repeated logic in netlists (such as would be synthesized from loops in the original HDL code) and rerolling them into syntactic loops in the recovered HDL code. This enables not only faster simulation, but also opens opportunities for transpilation between HDLs, compaction of netlists, understanding/analysis of netlists, and more.



Short Bio

Jonathan Balkind is an Assistant Professor in the Department of Computer Science at the University of California, Santa Barbara. His research interests lie at the intersection of Computer Architecture, Programming Languages, and Operating Systems. Jonathan completed his PhD and MA degrees at Princeton University and his MSci degree at the University of Glasgow. Jonathan was an Open Hardware Trailblazer Fellow and recipient of the NSF CAREER Award. Since 2021, he has served as a Director of the FOSSi Foundation.

Speakers

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Host: Miquel Moretó. High Performance Domain-Specific Architectures, Computer Sciences, BSC. Barcelona Supercomputing Center - Centro Nacional de Supercomputación

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