Hybrid SORS/LOCA Series: Deep Convolutional Neural Networks and Energy-efficient Hardware Acceleration

Objectives

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Abstract: Deep Convolutional Neural Networks (CNN) have achieved state-of-the-art inference accuracy in a wide range of computer vision applications like image classification, object detection, semantic segmentation etc. Applications based on CNN require millions of multiply-accumulate operations to be performed between input pixels and kernel weights during inference. Such CNNs when realized on embedded devices or edge devices of the Internet of Things, a power/energy-efficient compute platform is required, which needs to meet the limited power/energy budget of the devices. There have been numerous works in literature to address these requirements. With a brief introduction to CNNs, state-of-the-art CNNs and hardware accelerators this talk will highlight on challenges faced in the accelerators, and solutions. In addition, this talk refers to a few prior works by the presenter, with topics of interest for further research.

Short bio: Gopinath V. Mahale received his Bachelors in Electronics and communication engineering from the Visvesvaraya Technological University, India, in 2007, his Masters in electronics from the University of Pune, India, in 2011, and Ph.D. degree in electronic systems engineering from the Indian Institute of Science (IISc), Bangalore, India, in 2017. Currently he is a researcher at Barcelona Supercomputing Center (BSC). Prior to this he has worked as a Project Engineer at Wipro Technologies, as a Research Associate at the IISc, as a Postdoctoral Research Associate at the University of Paderborn, Germany and as a Staff Engineer at the Samsung Advanced Institute of Technology, SRIB, Bengaluru, India. His research interests include domain-specific hardware acceleration, machine learning, low power computations for deep learning, algorithm-architecture co-design and high-performance computing.

Speakers

Speaker: Gopinath Mahale, PhD., Group Established Researcher, Computer Sciences, European Exascale Accelerator
Host: Teresa Cervero, Leading Research Engineer, Computer Sciences, European Exascale Accelerator group

Barcelona Supercomputing Center - Centro Nacional de Supercomputación