

The Velox Transactional Memory Stack

Authors: [Felber](#), / [Rivière](#), / [Moreira](#), / [Harmanci](#), / [Marlier](#), / [Diestelhorst](#), / [Hohmuth](#), / [Pohlack](#), / [Cristal, Adrián](#) / [Hur, Ibrahim](#) / [Unsal, Osman](#) / [Stenström, Per](#) / [Dragojevic](#), / [Guerraoui](#), / [Kapalka](#), / [Gramoli](#), / [Drepper](#), / [Tomi?](#), [Sa?a](#) / [Afek](#), / [Korland](#), / [Shavit](#), / [Fetzer](#), / [Nowack](#), / [Riegel](#),

Publication: Micro, IEEE

Volume / Number / Pagination: 30 / 5 / 76 -87

Palabras clave: [atomic transaction](#), [compilers](#), [concurrency control](#), [concurrent programming](#), [fine grained locking](#), [Hardware](#), [hardware transactional memory](#), [integrated TM stack](#), [Java](#), [language extensions](#), [Libraries](#), [mainstream computing](#), [many-core architecture](#), [multicore architecture](#), [multiprocessing systems](#), [parallel architectures](#), [Parallel Programming](#), [Program processors](#), [Programming](#), [Runtime](#), [software transactional memory](#), [transactional memory programming](#), [Velox project design](#), [Velox TM stack](#), [Velox transactional memory stack](#)

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

Source URL (retrieved on 28 Sep 2024 - 10:32): <https://www.bsc.es/es/research-and-development/publications/the-velox-transactional-memory-stack>