

## [Sharing the Instruction Cache Among Lean Cores on an Asymmetric CMP for HPC Applications](#)

**Authors:** [Milic, Ugljesa](#) / [Rico, Alejandro](#) / [Carpenter, Paul](#) / [Ramirez, Alex](#)

**Research Lines:** [Microserver architectures and system software](#)

**Publication:** International Symposium on Performance Analysis of Systems and Software (ISPASS 2017)

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

---

**Source URL (retrieved on 13 Dic 2024 - 09:36):** <https://www.bsc.es/es/research-and-development/publications/sharing-the-instruction-cache-among-lean-cores-asymmetric-cmp>