

[Performance Impact of the Interconnection Network on MareNostrum Applications](#)

Authors: [Ramirez, Alex](#) / [Prat,](#) / [Labarta, Jesús](#) / [Valero, Mateo](#)

Publication: 1st Workshop on Interconnection Network Architectures: On-Chip, Multi-Chip (INA-OCMC 2007)

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

Source URL (retrieved on 18 Oct 2024 - 20:54): <https://www.bsc.es/es/research-and-development/publications/performance-impact-the-interconnection-network-marenostrum>