VELOX: An Integrated Approach to Transactional Memory on Multi- and Many-core Computers

Description

At the time of designing this project, the adoption of multi- and many-core chips as the architecture-of-choice for mainstream computing will undoubtedly bring about profound changes in the way software is developed. In particular, the use of fine grained locking as the multi-core programmer's coordination methodology is viewed by most experts as a dead-end. The transactional memory (TM) programming paradigm is a strong contender to become the approach of choice for replacing locks and implementing atomic operations in concurrent programming. Combining sequences of concurrent operations into atomic transactions promises a great reduction in the complexity of both programming and verification, by making parts of the code appear to be sequential without the need to program fine-grained locks. Transactions remove from the programmer the burden of figuring out the interaction among concurrent operations that happen to conflict when accessing the same locations in memory. To make TM an effective tool, TM systems needs the right hardware and software support to provide scalability not only in terms of number of cores, but also in terms of code size and complexity.

The objective of this project was to understand how to provide such support by developing an integrated TM stack. Such a TM stack would span a system from the underlying hardware to the high end application and would consist of the following components: CPU, operating system, runtime, libraries, compilers, programming languages and application environments. The anticipation was that such a fully integrated TM system will not only improve our understanding of TM designs but also greatly help in the adoption of the TM paradigm by the European software industry, making it a tool-of-choice for concurrent programming on multi- and many-core platforms. please refer to the project website for further details on the final deliverables.

Barcelona Supercomputing Center - Centro Nacional de Supercomputación