

## **MEEP: MareNostrum Experimental Exascale Platform**

### **Description**

The MareNostrum Experimental Exascale Platform (MEEP) is a flexible FPGA-based emulation platform that will explore hardware/software co-designs for Exascale Supercomputers and other hardware targets, based on European-developed IP. MEEP provides two very important functions:

- An evaluation platform of pre-silicon IP and ideas, at speed and scale and
- A software development and experimentation platform to enable software readiness for new hardware.

MEEP enables software development, accelerating software maturity, compared to the limitations of software simulation. IP can be tested and validated before moving to silicon, saving time and money. The objectives of MEEP are to leverage and extend projects like EPI and the POP2 CoE in the following ways:

- Define, develop, and deploy an FPGA-based emulation platform targeting European-based Exascale Supercomputer RISC-V-based IP development, especially hardware/software co-design.
- Develop a base FPGA shell that provides memory and I/O connectivity to the host CPU and other FPGAs.
- Build FPGA tools and support to map enhanced EPI and MEEP IP into the FPGA core, validating and demonstrating European IP.
- Develop the software toolchain (compiler, debugger, profiler, OS, and drivers) for RISC-V based accelerators to enable application development and porting.

MEEP will deliver a series of Open-Source IPs, when possible, that can be used for academic purposes and integrated into a functional accelerator or cores for traditional and emerging HPC applications. This is an exciting target for IPs generated from projects like EPI, and an IP source for follow-on projects as well. MEEP will provide a foundation for building European based chips and infrastructure to enable rapid prototyping using a library of IPs and a standard set of interfaces to the HostCPU and other FPGAs in the system using the FPGA shell. In addition to RISC-V architecture and hardware ecosystem improvements.

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