Exanode: European Exascale Processor Memory Node Design

Description

ExaNoDe will develop and pilot (technology readiness level 7) a highly efficient, highly integrated, multi-way, high performance, heterogeneous compute element aimed towards exascale computing and demonstrated using hardware emulated interconnect. It will build on multiple European initiatives for scalable computing, utilizing low-power processors and advanced nanotechnologies. ExaNoDe will draw heavily on the Unimem memory and system design paradigm defined within the EUROSERVER FP7 project, providing low-latency, high-bandwidth and resilient memory access, scalable to Exabyte levels. The ExaNoDe compute element aims towards exascale compute goals through:

- Integration of the most advanced low-power processors and accelerators across scalar, SIMD, GPGPU and FPGA processing elements supported by research and innovation in the deployment of associated nano-technologies and in the mechanical requirements to enable the development of a high-density, high-performance integrated compute element with advanced thermal characteristics and connectivity to the next generation of system interconnect and storage;
- Undertaking essential research to ensure the ExaNoDe compute element provides necessary support of HPC applications including I/O and storage virtualization techniques, operating system and semantically aware runtime capabilities and PGAS, OpenMP and MPI paradigms;
- The development an instantiation of a hardware emulation of interconnect to enable the evaluation of Unimem for the deployment of multiple compute elements and the evaluation, tuning and analysis of HPC mini-apps.

Each aspect of ExaNoDE is aligned with the goals of the ETP4HPC. The work will be steered by first-hand experience and analysis of high-performance applications, their requirements and the tuning of their kernels.

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