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Description

The number and diversity of embedded FPGA SoC (System On Chip) in modern satellites is increasing and so it is the complexity and cost to use them efficiently and safely. With the emergence of these platforms, software architects and developers are facing increasingly difficult challenges to (i) optimize the deployment of software to efficiently use the available resources, (ii) comply with the applicable safety and availability constraints, and (iii) increase software development productivity. Programming languages traditionally used in critical real-time systems have not been designed to address the extreme parallelism of modern platforms. To address this limitation, OpenMP, the de-facto standard for exploiting parallel and heterogeneous processor architectures in the HPC domain, is increasingly being considered a suitable solution to expose and exploit parallelism in SoCs currently used in critical domains. OpenMP implements a comprehensive set of computation models (e.g., loop and task parallelism), comes with a very large set of assets (e.g., tools, libraries), and supports a large set of CPU and accelerator devices (e.g., GR740, MPPA, NVIDIA Jetson and Xilinx Ultrascale+). Despite preliminary analysis has proven the productivity and efficiency of OpenMP in the space, automotive and railway domains, there are some challenges to be addressed. Therefore, our proposed solution is based on an advanced OpenMP framework that combines an enhanced parallel programming model, with adapted compiler and runtime systems. This new OpenMP system aims to provide benefits along two axes: - Resilience: Take advantage of the parallel and heterogeneous capabilities of the newest SoCs to leverage productivity on software fault-tolerance techniques like replication, N-version programming and monitoring. - Efficiency: Providing techniques to facilitate the design space exploration of multiple deployment configurations towards CPUs, GPUs and FPGAs in the newest space SoCs.

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

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