eProcessor: European, extendable, energy-efficient, energetic, embedded, extensible, Processor Ecosystem

Description

The eProcessor ecosystem combines open source software (SW) and hardware (HW) to deliver the first completely open source European full stack ecosystem based on a new RISC-V CPU coupled to multiple diverse accelerators that target traditional HPC and extend into mixed precision workloads for High Performance Data Analytics (HPDA), (AI, ML, DL andBioinformatics). eProcessor will be extendable (open source), energy-efficient (low power), extreme-scale (high performance), suitable for uses in HPC and embedded applications, and extensible (easy to add on-chip and/or off-chip components), hence, the e used as a wild card in eProcessor proposal name.

eProcessor combines cutting edge research utilizing SW/HW co-design to achieve sustained processor and system performance for (sparse and mixed-precision) HPC and HPDA workloads by combining a high performance low power (architecture and circuit techniques) out-of-order processor core with novel, adaptive on-chip memory structures and management, as well as fault tolerance features. These software-hardware co-design solutions span the full stack from applications to runtimes, tools, OS, and the CPU and accelerators. eProcessor is able to pursue a full stack (SW and HW) research project by leveraging and extending the work done in multiple European projects like: European Processor Initiative, Low-Energy Toolset for Heterogeneous Computing, MareNostrum Experimental Exascale Platform, POP2 CoE, Tulipp, EuroEXA and ExaNeSt. By doing so, we can improve the Technical Readiness Level (TRL) and work with industrial partners that provide a direct path to commercialization. This can only be done with a combination of SW simulation, HW emulation using FPGAs, and real ASIC prototypes that demonstratethe full stack feasibility of the hardware and software. Finally, while the applications we use span IoT to HPC, the ASIC implementation will be in a technology node that can easily be adopted for a near-future HPC implementation.

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