

## [Deconstructing Bus Access Control Policies for Real-Time Multicores](#)

**Authors:** [Jalle, Javier](#) / [Abella, Jaume](#) / [Quinones, Eduardo](#) / [Fossati, Luca](#) / [Zulianello, Marco](#) / [Cazorla, Francisco](#)

**Teams:** [Computer Architecture - Operating Systems \(CAOS\)](#)

**Publication:** 8th IEEE International Symposium on Industrial Embedded Systems (SIES)

**Place Published:** Porto, Portugal

**Pagination:** 31?38

**Palabras clave:** [authorisation](#), [Benchmark testing](#), [bus access control policy](#), [bus contention-control policy](#), [critical real-time system](#), [Delays](#), [Embedded systems](#), [Hardware](#), [IABA policy](#), [interference-aware bus arbiter policy](#), [Multicore processing](#), [multiprocessing systems](#), [Program processors](#), [Real-time systems](#), [realtime multicore system](#), [TDMA policy](#), [Time division multiple access](#), [time-division multiple access policy](#), [WCET estimation](#), [worst-case execution time](#)

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

---

**Source URL (retrieved on 15 Jul 2024 - 13:51):** <https://www.bsc.es/es/node/40594>