

Parallelizing general histogram application for CUDA architectures

Authors: [Milic, Ugljesa](#) / [Gelado, Isaac](#) / [Puzovic, Nikola](#) / [Ramirez, Alex](#) / [Tomasevic, Milo](#)

Publication: 2013 International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS XIII)

Place Published: Samos, Greece

Pagination: 11?18

Palabras clave: [Algorithm design and analysis](#), [CUDA architectures](#), [Histograms](#), [optimal algorithm](#), [parallel architectures](#)

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

Source URL (retrieved on 30 Abr 2025 - 14:18): <https://www.bsc.es/es/node/40578>