RISC-V: the cornerstone ISA for the next generation of HPC infrastructures

BSC and E4 Computer Engineering co-organise this Workshop on RISC-V at HIPEAC 2024.

The workshop will bring together researchers from different disciplines, representatives from industries, computer architects, developers of scientific applications and users to describe the state of the art and outline the paths to be taken by RISC-V to make it the preferred ISA for HPC applications.

Co-design is a tremendous opportunity for fostering collaborations among the developers of application, hardware architects, data centres and users.
Co-design will impact all scales of computing from desktops to supercomputers because all these scales face similar challenges in performance, energy efficiency, concurrency, data movement and application's programmability.
For RISC-V in large HPC infrastructures, there will be additional challenges including scalability and reliability that are brought about by the extreme size of such systems. The workshop will provide a lively discussion and present early experiences and use cases of HPC infrastructure powered by RISC-V platforms.

Further information here: https://www.hipeac.net/2024/munich/#/program/sessions/8088/

- Collocated with HiPEAC Conference 2024

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

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