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Objectives

The 3rd HMEM workshop serves as a forum to present and discuss ongoing research around heterogeneous memory systems. The scope of the workshop encompasses all the layers of system and software stack, from computer architectures, operating system, middleware, programming models, runtime systems, tools, to applications.

Collocated with ICS2022

• Submissions: https://easychair.org/account/signin?l=cXqqxy1iTNkOHCP9gLh6rC

VIDEOS

If you missed the workshop or you want to recover it, follow these links:

- https://youtu.be/WHHfk_GiThM
- https://youtu.be/gKYhC3X03Jw
- <u>https://youtu.be/0mpbDQbFbnU</u>

Heterogeneous memory architectures have recently emerged and revolutionized the traditional memory hierarchy. Today's architectures may comprise multiple memory nodes, organized in complex non-uniform access (NUMA) topologies, whose nodes include not just DRAM, but also die-stacked DRAM, high-bandwidth multi-channel RAM, or persistent memory.

By combining different memory technologies, heterogeneous memory architectures allow today's systems to take advantage of the strengths of each technology — namely, in terms of latency, bandwidth, capacity, persistence or cost. As a result, applications may benefit from improved performance, energy-efficiency, and cost trade-offs.

Still, exploiting the full potential of heterogeneous memory architectures poses significant challenges. Since heterogeneous memory architectures introduce dramatic disruptions to the usual memory hierarchy assumptions that have guided decades of system and software design, we need to rethink the full system stack to embrace the new era of memory heterogeneity.

Following a successful inaugural edition at ICS 2020, the 2nd HMEM workshop will serve as a forum to present and discuss ongoing research around heterogeneous memory systems. The scope of the workshop encompasses all the layers of system and software stack, from computer architectures, operating system, middleware, programming models, runtime systems, tools, to applications.

Topics of interest include, but are not limited to:

- Data allocation and placement in heterogeneous memories
- Caching for heterogeneous memories
- Software-defined far memories
- Disaggregated memory
- New memory consistency and persistency models
- Persistent data structures
- Abstractions and support for failure-atomicity in persistent memory
- Use cases and early experiences

Prospective authors must submit an extended abstract of up to 4 pages through EasyChair. Extra pages can be included in a clearly marked appendix (to be read at the discretion of the reviewers). The extended abstract should include author names (single-bllind review) and use the ACM proceedings template (https://www.acm.org/publications/proceedings-template).

Prospective speakers are also welcome to submit extended abstracts based on their recent publications.

This is a traditional-style workshop without formal papers or proceedings. The authors of accepted communications will be invited to (optionally) upload their extended abstract (PDF) for publication on the workshop website.

- Submission deadline: June 3, 2022 (AOE).
- Acceptance notification: June 10, 2022

General Chairs:

Joao Barreto, INESC-ID, Universidade de Lisboa

Antonio J. Peña, Barcelona Supercomputing Center (BSC)

Harald Servat, Intel

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

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