# RoMoL 2016 brings together the best computer architects to Barcelona

After the workshop, UPC and BSC will organise a homage event for our late colleague Nacho Navarro.

On 17 and 18 March, some of the top researchers in computer architecture converged in Barcelona to participate at Riding on Moore Law's – RoMoL 2016 Workshop. The event brings together internationally recongnized researchers in this field, including five winners of the prestigious Eckert Mauchly award

(popularly known as the Nobel for computer architecture). These distinguished researchers and industry representatives in the field of computer sciences have in some way collaborated or have been in contact with BSC, UPC, the FIB's Computer Architecture department, and the former CEPBA. Conference sessions centred on topics such as computer architecture, runtime systems and programming models will enable discussions on how to achieve strengthened co-operation and improved interoperability and co-design opportunities between the runtime system and the underlying hardware.

After the workshop, on Friday afternoon, UPC and BSC will organise a homage event for our late colleague Nacho Navarro. The memorial event will take place Friday 18 at 15:00, in Vertex building, just after the RoMoL 2016 Workshop. It will consist of many small interventions, with sharings, experiences, anecdotes that many people have had with Nacho along all these years. More information can be found here: http://inmemoriam.bsc.es/.

See more photos here.
Photos of the homage event here.

Nacho Navarro
1958 - 2016
Born in Barcelona
Studied in Liceu Frances and Universitat Politecnica de Catalunya
PhD in Computer Science
Expert in operating systems, enjoyed the internals of UNIX, Mach, Chorus, Exokernels
Associate Professor at DAC (UPC)
Leader of the group Accelerators for HPC (BSC)
Participated in multiple European Projects
Organizer of PUMPS Summer School
Co-organizer of many events within HiPEAC
Visiting Professor of the IMPACT group (CSL-UIUC)
Leader of the BSC/UPC NVIDIA GPU CoE
Memorial Event: Friday 15:00 UPC, Vertex Building
UPC

Optimizing resources at run time
Some of the work we have done
MorphCore (Khubaib, IEEE/ACM Micro 2012)
Adaptive Processors, (Miftakhudinov, Micro 2012)
Shared resources (IEEE/ACM ISCA 2012)
Which thread to speed up (Joao, ISCA 2013)
Enhanced memory controller (Hashemi, ISCA 2016)
All depend on knowing chip_resources/utilization
Can we do more?
UPC

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

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