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Parallel Software Framework for Time-Critical many-core Systems

<u>P-SOCRATES</u> (Parallel Software Framework for Time-Critical Many-core Systems) will allow current and future applications with high-performance and real-time requirements to fully exploit the huge performance opportunities brought by the most advanced many-core processors, whilst ensuring a predictable performance and maintaining (or even reducing) development costs of applications. The purpose of P-SOCRATES is to develop an entirely **new design framework, from the conceptual design of the system functionality to its physical implementation, to facilitate the deployment of standardized parallel architectures in all kinds of systems. The technology developed within P-SOCRATES will be evaluated within different system scenarios provided by project advisory board members.**

"There is a real necessity of new tools for the software development of parallel systems", said Dr. Claudio Scordino, of Evidence, the SME responsible for the operating system development. "P-SOCRATES will provide an entirely new generic design framework, from the conceptual design of the system functionality to its physical implementation, to facilitate the deployment of standardized parallel architectures in all kinds of systems", he concluded.

"The computing technology developed in the project will allow a deeper understanding of many-core off-theshelf processors, enabling new kinds of applications to be developed on top of such platforms", added Dr. Michele Ramponi, of Active Technologies, provider of the hardware platform, build upon a many-core processor from the advisory board member STMicroelectronics.

Nowadays, the prevalence of electronic and computing systems in our lives is so ubiquitous that it would not be far-fetched to state that we live in a cyber-physical world dominated by computer systems. Examples include pacemakers implanted within the human body to regulate and monitor heartbeats, cars and airplanes transporting us, smart grids and traffic management.

All these systems demand for more and more computational performance to process large amounts of data from multiple data sources, and some of them with *guaranteed processing response times*. In other words, systems required to deliver their results within pre-defined (and sometimes extremely short) time bounds. This *timing aspect* is vital for systems like planes, cars, business monitoring, e-trading, etc. Examples can be found for instance in intelligent transportation systems for fuel consumption reduction in cities or railway, or autonomous driving of vehicles. All these systems require processing and actuation based on big amounts of data coming from real-time sensor information.

As a result, the computer electronic devices to which these systems depends on are constantly required to become more and more powerful and reliable, while remaining affordable. In order to cope with such performance requirements, chip designers have recently started producing chips containing multiple processing units, the so called *multi-core processors*, effectively integrating multiple computers within a single chip, and more recently the *many-core processors*, with dozens or hundreds of cores, interconnected with complex networks on chip. This radical shift in the chip design paved the way for parallel computing: rather than processing the data sequentially, the cooperation of multiple processing elements within the same chip allowed systems to be executed concurrently, *in parallel*.

Unfortunately, the parallelization of the computing activities brought upfront many challenges, because it affects the timing behavior of systems as well as the entire way people think and the design computers: from the design of the hardware architecture, through the operating system up to the conceptualization of the enduser application. Therefore, although multi-core processors are promising candidates to improve the responsiveness of these systems, the interactions that the different computing elements may have within the chip, can seriously affect the performance opportunities brought by parallel execution. Moreover, providing timing guarantees becomes harder, because the timing behavior of the system running within a multi-core processor depends on interactions that are most of the time not know by the system designer. This makes system analysts to be struggled trying to provide timing guarantees for such platforms. Finally, most of the optimization mechanisms buried deep inside the chip are geared only to increase performance and execution speed rather than providing predictable time behavior.

"P-SOCRATES brings together world-class researchers, with the complementary expertises required to tackle these complex challenges. P-SOCRATES will represent a reference point for the implementation of real-time complex event-processing systems, and, more in general, of workload-intensive applications with time-criticality requirements", said Dr. Luis Miguel Pinho, the Project Coordinator.

The P-SOCRATES consortium exploit synergies and strengths between different computing segments to successfully address the challenge of exploiting the performance opportunities brought by the newest many-core processors currently available in the market. To that end, the project brings together teams from the

high-performance (Barcelona Supercomputer Center and Atos), embedded (Swiss Federal Institute of Technology Zurich and Active Technologies) and real-time (Instituto Superior de Engenharia do Porto, University of Modena and Evidence) computing segments, in a stack that ranges from the application provider to the hardware manufacturer.

The project partners are supported by a broad advisory board of multi-national companies, high-tech SMEs and application providers. This board, which includes STMicroelectronics, IBM, Honeywell, Airbus, Expert Systems, Rapita Systems, and the council of the City of Bratislava, will both give advice on the project progress as well as act as end users of the P-SOCRATES technology.

More information available from www.p-socrates.eu

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