Inicio > LG Electronics uses BSC programming model OmpSs
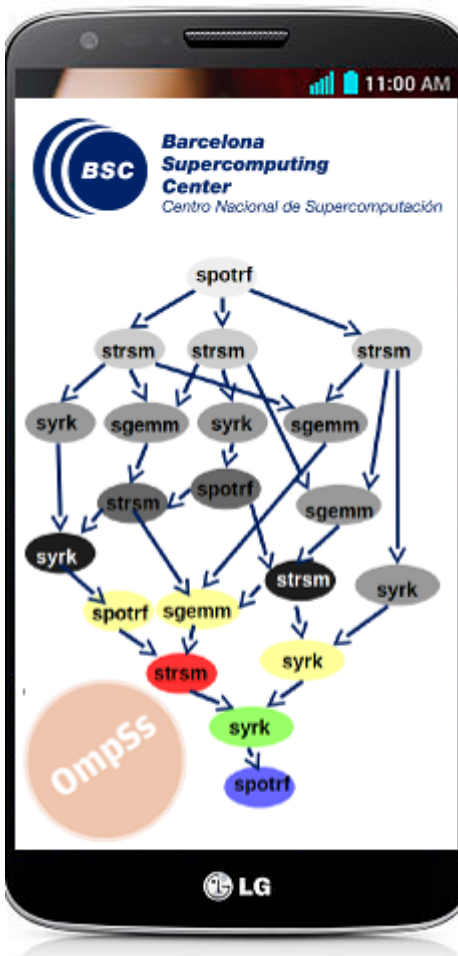
LG Electronics uses BSC programming model OmpSs

BSC is collaborating with LG Electronics to improve the software part of the runtime in order to further increase the TGA hardware capabilities for their specific target market.

LG Electronics is developing a hardware implementation to support OpenMP 4.0 and the OmpSs programming model developed by the BSC Computer Sciences Department, as presented at the Hot Chips conference by LG. In this event, LG Electronics has followed the principle of using a hardware accelerator for "Task Graph Acceleration" (TGA), which enables tasking with minimum overhead. This path was opened up by Task Superscalar and Picos, BSC's own hardware implementations of TGA that have also showed great potential for many-core systems.

"The fact that LG Electronics targets our programming model OmpSs is a great opportunity to raise awareness about its incredible features in markets other than the HPC sector.", says Jesús Labarta, BSC Computer Sciences Director.

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increase the TGA hardware capabilities for their specific target market.

Over 20 years of experience developing programming models

With over 20 years of broad experience in developing programming models, BSC has a Programming Models research group whose aim is to investigate programming paradigms towards productive programming and their implementation through intelligent runtime systems that effectively exploit performance out of the target architecture. This team is continuously looking to improve their models by releasing new versions, creating new hardware to help exploit its potential and teaching the features of models to the HPC community.

Interested in knowing more about BSC's programming model? Talk to one of our experts by sending an email to pm-tools[at]bsc.es or visit the website: https://pm.bsc.es/ompss.

Related Scientific papers

Xubin Tan, J. Bosch, D. Jiménez-González, C. Álvarez-Martínez, E. Ayguadé and M. Valero, "Performance analysis of a hardware accelerator of dependence management for task-based dataflow programming models," *2016 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, Uppsala, 2016, pp. 225-234. DOI: 10.1109/ISPASS.2016.7482097

Fahimeh Yazdanpanah, Carlos Álvarez, Daniel Jiménez-González, Rosa M. Badia, and Mateo Valero. 2015. Picos. *Future Gener. Comput. Syst.* 53, C (December 2015), 130-139. DOI: http://dx.doi.org/10.1016/j.future.2014.12.010

Yoav Etsion, Felipe Cabarcas, Alejandro Rico, Alex Ramirez, Rosa M. Badia, Eduard Ayguade, Jesus Labarta, and Mateo Valero. 2010. Task Superscalar: An Out-of-Order Task Pipeline. In*Proceedings of the 2010 43rd Annual IEEE/ACM International Symposium on Microarchitecture*(MICRO '43). IEEE Computer Society, Washington, DC, USA, 89-100. DOI=http://dx.doi.org/10.1109/MICRO.2010.13

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