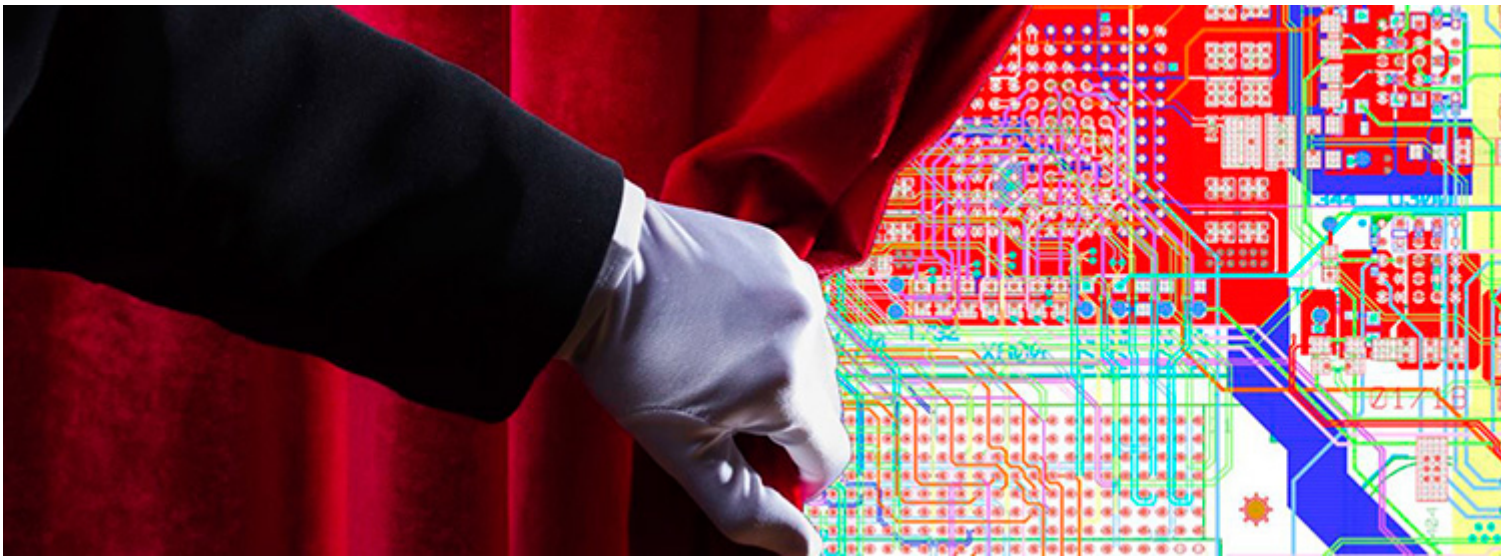
dReDBox presents its novel Board Management Controller



The European project dRedBox, in which Barcelona Supercomputing Center (BSC) participates, has presented its Board Management Controller (dBMC). dBMC is a special dedicated computer whose role is to manage the compute, memory and accelerator resources available in the tray of an unconventional data centre built from disaggregated resources.

The dBMC is built from off-the-shelf hardware: a Xilinx Zynq UltraScale+ MPSoC, with 4 GiB Micron DDR4 SDRAM (ECC protected) and a 64 MiB Micron QSPI Flash. Other features include an upgradable SD-card flash storage, 16 high speed transceiver channels (up to 16Gb/s) and a Samtec SEARAY™ connector.

As BSC researcher, **Ferad Zyulkyarov** explains: “the trays that today’s data centres are built of are off-the-shelf computers which run complete SW stack. They might have board management computer (BMC) but its role is very different from the role of the dBMC in dRedBox tray. Unlike traditional data centres, in dRedBox, we split and disaggregate the resources of monolithic computers into CPU, memory and accelerator nodes”.

In addition, **Zyulkyarov** adds that “because these nodes cannot run a full software stack and manage themselves, their management is offloaded to a dedicated computer, the Board Management Controller (dBMC). Each dRedBox tray consists of numerous dRedBox nodes (CPU, memory or accelerators) and one dBMC, which manages these nodes. The dBMC powers the nodes on/off, configures the connections between the nodes, and performs monitoring operations”.

BSC has been responsible for implementing the software layer, REST API, through which the dBMC firmware can be accessed via a standard WebAPI interface. The REST API is used by standard data centre software such as OpenStack to control and manage the nodes on the tray.

The goal of the dReDBox project is to build a novel prototype data centre architecture and system based on disaggregated compute, memory and accelerator nodes. BSC has a leading role in the design and the

implementation of this prototype dRedBox system. Unlike conventional architectures, in dRedBox, components such as CPU, memory and accelerators are decoupled and a data centre build based on dRedBox can be flexibly extended by just buying nodes that only have a CPU or nodes that only have memory or nodes which only have accelerators.

The CPU, memory and accelerator nodes have compatible interfaces, making them interchangeable. For example, it is possible to unplug a memory node and plug in a CPU node in its place. In the dRedBox design, the CPU, memory and accelerator nodes are inserted (plugged) into a main circuit board, which is called a tray. With the release of the dBMC, the tray now has a special component with functions including turning CPU, memory and accelerator nodes on and off, connecting one CPU node with a memory node and monitoring the health of the nodes.

About dReDBox

The dReDBox consortium features a versatile set of prominent European R&D organizations, including Barcelona Supercomputing Center (Spain), IBM Research (Ireland), Telefonica (Spain), UCL (UK), University of Thessaly (Greece), the Foundation for Research and Technology (Greece), Naudit (Spain), Sintecs (Netherlands), Virtual Open Systems (France) and Kinesense (Ireland). The project started in January 2016 and is planned to finish on December 2018, funded by EC Horizon 2020 programme with a budget of €6 million.

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