BSC at DATE 2016

The 20th edition of the DATE conference is taking place in Dresden (Germany) from 14 to 18 March and BSC is participating in multiple events and activities.

The DATE conference and exhibition is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems. It puts strong emphasis on both ICs/SoCs, reconfigurable hardware and embedded systems, including embedded software.

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BSC is present in 5 out of the 10 European project booths:

- PROXIMA - Probabilistic real-time control of mixed-criticality multicore and manycore systems: booth EP 1
- EuroSERVER - Green Computing Node for European Micro-servers: EP 5
- EuroLab-4-HPC - Foundation for a Centre of Excellence in High-Performance Computing Systems: EP 5
- ExaNoDe - European Exascale Processor Memory Node Design: EP 6
- SAFURE - Safety and Security by design for interconnected mixed-critical cyberphysical systems: EP 7

BSC is also present in the HiPEAC booth, no. 10, attending questions about HiPEAC's activities in high-performance and embedded systems research, jobs mobility, recruitment and more.

BSC's Operating System Group Manager Francisco Cazorla is the chair of the session "Enhancing Memory in Next-Generation Platforms" taking place on Thursday, 17 March. This session presents three interesting papers describing different approaches for enhancing memory in order to obtain significant performance and energy improvements with respect to standard processor-centric architectures.

Dr Cazorla, on behalf of PROXIMA project, is also co-organising the workshop "W04 IMPAC: Getting more for less: Innovative MPSoC Architecture Paradigms for Analysability and Composability of Timing and Power". This workshop aims at presenting and discussing the latest research results within this spectrum of topics, with emphasis on new on-chip architectures and analysis paradigms to enable fast, yet accurate, and dependable analysis, to support the incremental integration of heterogeneous applications in MPSoCs.

BSC will also participate in the technical programme, presenting the following papers:

- A Detailed Methodology to Compute Soft Error Rates in Advanced Technologies
  Marc Riera, Ramon Canal, Jaume Abella and Antonio Gonzalez
- Supertask: Maximizing Runnable-level Parallelism in AUTOSAR Applications

Sebastian Kehr, Miloš Pani?, Eduardo Quiñones, Bert Böddeker, Jorge Becerril Sandoval, Jaume Abella, Francisco J. Cazorla and Günter Schäfer

- Improving Performance Guarantees in Wormhole Mesh NoC Designs
  Miloš Pani?, Carles Hernandez, Jaume Abella, Antoni Roca, Eduardo Quiñones y and Francisco J. Cazorla
- Response-Time Analysis of DAG Tasks under Fixed Priority Scheduling with Limited Preemptions
  Maria A. Serrano, Alessandra Melani, Marko Bertogna and Eduardo Quiñones
- Rack-scale Disaggregated Cloud Data Centers: The dReDBox Project Vision
  K. Katrinis, D. Syrivelis, D. Pnevmatikatos, G. Zervas, D. Theodoropoulos, I. Koutsopoulos, K. Hasharoni, D. Raho, C. Pinto, F. Espina, S. Lopez-Buedo, Q. Chen, M. Nemirovsky, D. Roca, H. Klos and T. Berends
- EUROSERVER: Share-Anything Scale-Out Micro-Server Design
  Manolis Marazakis, John Goodacre, Didier Fuin, Paul Carpenter, John Thomson, Emil Matus, Antimo Bruno, Per Stenstrom, Jerome Martin, Yves Durand and Isabelle Dor

- Energy Minimization at All Layers of the Data Center: The ParaDIME Project
  Oscar Palomar, Santhosh Rethinagiri, Gulay Yalcin, Ruben Titos-Gil, Pablo Prieto, Emma Torrella, Osman Unsal, Adrian Cristal, Pascal Felber, Anita Sobe, Yaroslav Hayduk, Mascha Kurpicz, Christof Fetzer, Thomas Knauth, Malte Schneegaß, Jens Struckmeier and Dragomir Milojevic

Two BSC PhD students are attending the PhD Forum, Milos Panic and Leonidas Kosmidis. Kosmidis is presenting Enabling Caches in Probabilistic Timing Analysis, who has been nominated as best PhD student of this forum.


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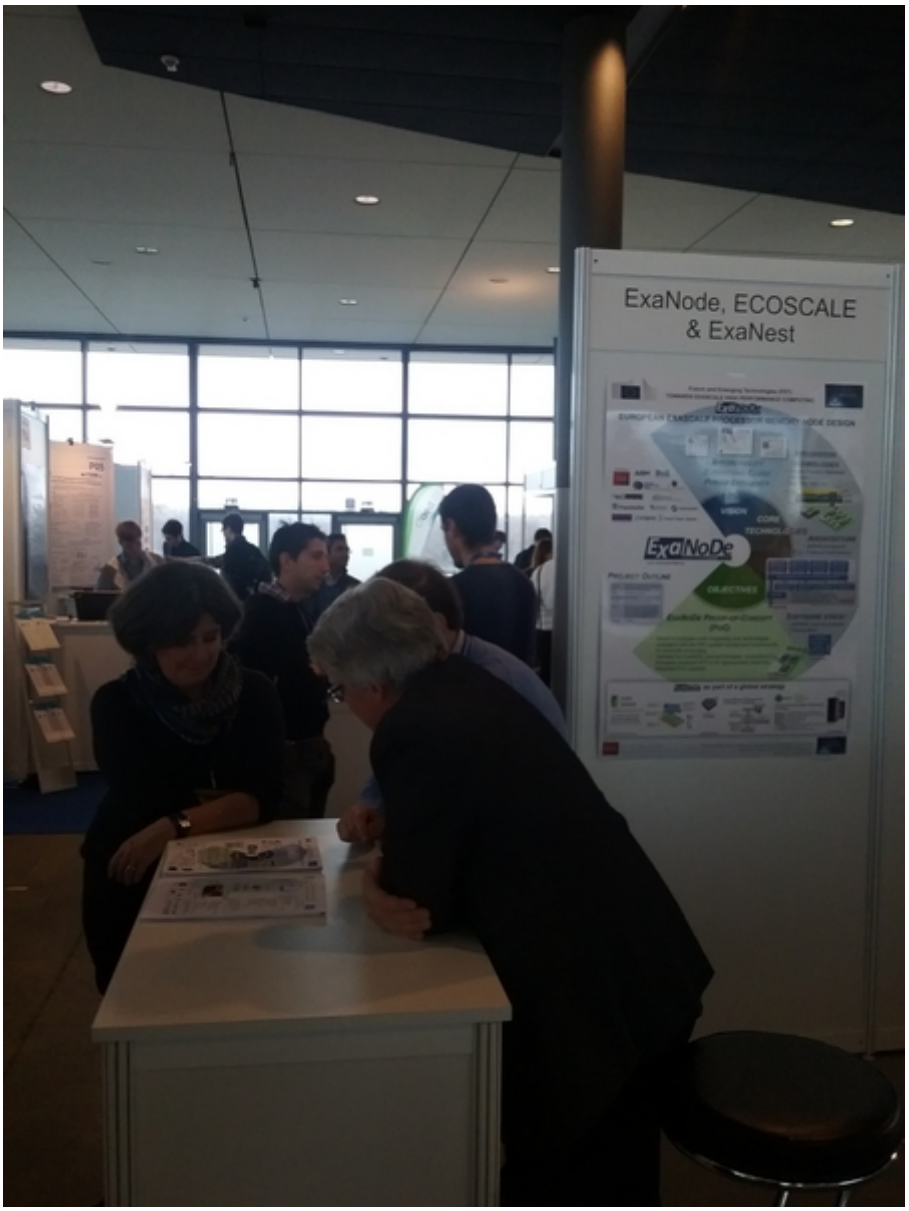

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