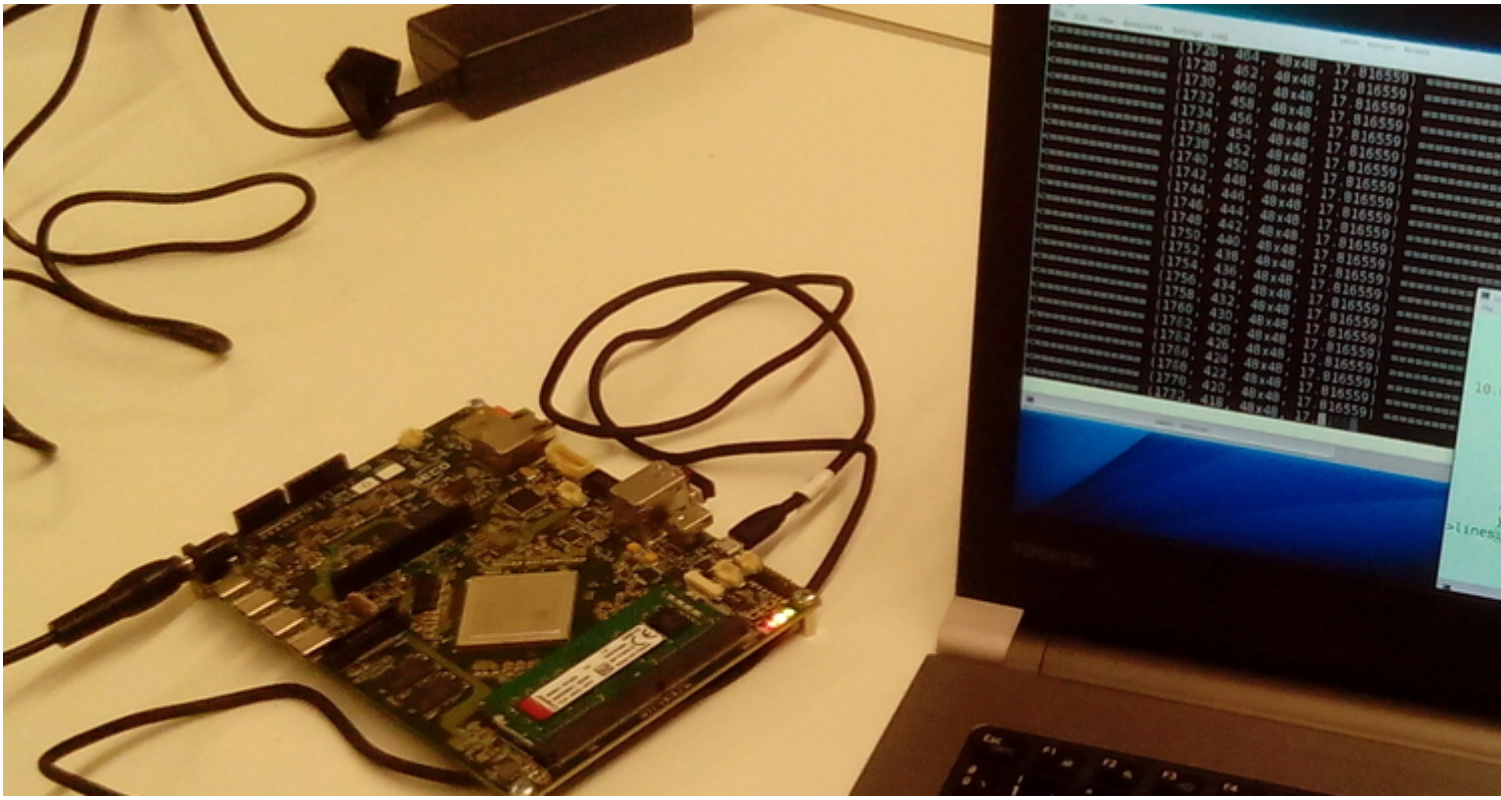
BSC and HERTA SECURITY boot AXIOM board for the first time and run algorithms successfully



As part of the European project called AXIOM, Computer science researchers from the Barcelona Supercomputing Center and Herta Security – a company that provides security tools focusing on facial recognition technologies - met in Barcelona on 17 March to test the first boot of the AXIOM board. Not only the boot was successful, the team could run the Herta face detection algorithm and tested OmpSs@SMP, which also run successfully on the YUV to RGB color space conversion.

The AXIOM board combines three worlds in one: Arduino, ARM 64-bit computing and FPGA. It is produced by SECO, and based on the Xilinx Ultrascale+ chip. The tests, in line with the initial plans on the adoption of OmpSs on users' own applications, have been carried out with the SECO ecosystem software and the OmpSs programming model developed by BSC.

As Xavier Martorell, Parallel Programming Models Group Manager at BSC, explains, "from now on, we start the most interesting phase of the AXIOM project, where we should demonstrate how useful the FPGA of the Ultrascale+ is to accelerate these algorithms". Martorell also shares that they are confident in being able to present these results in the next months in scientific environments.

Booting the AXIOM board and deploying successfully these initial tests are a significant step forward for the project and open the possibility to develop much further the outputs, impact and results of the project.

David Oro of Herta Security believes reconfigurable low-power SoCs such as the one included in the

AXIOM board will play a major role in the future for implementing neural network and machine learning video analytics algorithms for the surveillance industry: "Historically, the problem with FPGAs has been the difficulty on architecting high-performance designs under the pressure of tight product development schedules. The OmpSs@FPGA programming model developed by BSC enables us to quickly port and parallelize our algorithms for FPGA architectures with minimal source code modifications".

About the AXIOM board

This board has been developed in the framework of the European project AXIOM (Agile, eXtensible, fast I/O Module for the cyber-physical era).

The board presents the same pinout of Arduino Uno, so to let you attach an Arduino Uno-compatible shield to the board. In addition, the presence of Arduino UNO pinout enables fast prototyping and exposes the FPGA I/O with a user-friendly interface. The ARM computer on board consists in a 6-core heterogeneous processor – a 64-bit Quad core A53 @ 1.2GHz and a 32-bit Dual core R5 @ 500MHz, produced by Xilinx. The FPGA fabric is a new-generation Zynq Ultrascale Plus. The combination of a powerful heterogeneous 6-core ARM processor with a flexible and fast connection unleashes the true potential of the FPGA.

The AXIOM Board is, in other words, designed to be the perfect combination of High-Performance Computing, Embedded Computing and Cyber-Physical Systems.

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*** Caption:***The HERTA application executing with OmpSs on the AXIOM board*

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