BSC Training Course: RISC-V principles for understanding how to freely develop new solutions

Objectives

RISC-V is an open instruction set standard which is experiencing extraordinary growth all over the world in numerous areas of focus ranging from HPC & ML to the data center to embedded computing. The standardization activities are community driven by expert members (from industry, academia and individuals). BSC is one of the community members that is contributing to the ecosystem. This course is an opportunity to get familiar with technical aspects of the standard through a combination of lectures and hands-on sessions.

This course identifies topics that are both fundamental to computer architecture and relevant to the design of RISC-V based solutions of the future. The emphasis is always on insights that will be useful to the (under)graduate student, whether he/she goes on for a PhD or joins a software or hardware development team. We will deal with principles, trade-offs, and implementation details related to the RISC-V standard. Along the course, the students will get familiar with some layers of the RISC-V software and hardware stacks using a learning-by-doing methodology. This will provide a mechanism to the students to understand the RISC-V ecosystem, BSC know-how and activities related to RISC-V, and explore the potential of the ISA to freely develop new technologies..

Topics will cover aspects like: how to boot an operating system, how to deploy a container and execute an application, how to tune an algorithm for improving its performance through the addition of custom instructions, and finally, how to improve the performance of an HPC application by taking advantage of the RISC-V Vector extension.

Requirements

Prerequisites: Being familiar with the installation of a VMN, basic skills in C/C++ programming language, basic understanding of assembly. Some experience with QEMU is a plus, but not required. Students need to bring their own laptop for the practical sessions.

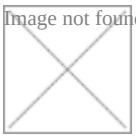
Learning Outcomes

Participants will get familiar with basic concepts in RISC-V ISA and its extensions; learn about the RISC-V ecosystem, focused on the open-source stack, going through software and hardware layers. Afterward, they will be directed to self-guided HPC challenges covering basic data parallelism and vector computation.

More precisely, the course will cover:

- RISC-V Fundamentals and ecosystem.
- RISC-V activities at BSC
- Identifying particularities of the booting process in RISC-V
- Learning how to boot an OS on a RISC-V architecture (reset vector, bootrom, firmware OpenSBI, and differences between Machine, Supervisor and User mode, basic I/O (uart, Pmem)
- Virtualization with PyTorch and Singularity
- Designing and implementing new RISC-V instructions (custom instructions) as an opportunity for optimizing a solution
- Understanding the difference between emulating (QEMU) and simulating (Gem5) a RISC-V architecture
- Understanding the popular RVV (RISC-V Vector Extension)
- Exploiting data-level parallelism using vector computation (RVV)
- Using QEMU for emulating a RISC-V platform.

Academic Staff



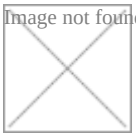
Course Convener: Teresa Cervero, Computer Science Department - Technical Management Hardware Engineering Group. Leading Research Engineer

Lecturers:

BSC - Computer Sciences department

Teresa Cervero - Computer Science - Technical Management HW engineering. Leading research engineering
Xavier Martorell - Computer Sciences - Programming Models. Group manager and professor at UPC
Aaron Call - Computer Science - Data Centric Computing. Established researcher
Julián Pavón - Computer Science - Computer Architecture for Parallel Paradigms. Research Engineer
Filippo Mantovani - Computer Sciences - Mobile and embedded-based HPC. Established Researcher
Roger Ferrer - Computer Sciences - Compilers and Toolchains for HPC. Senior Research Engineer
Pablo Vizcaino - Computer Sciences - Mobile and embedded-based HPC. Junior Research Engineer
Ivan Vargas - Computers Sciences - Computer Architecture for Parallel Paradigms. Research Engineer

Materials



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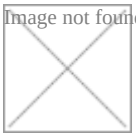
Further information



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PLEASE BRING YOUR OWN LAPTOP.

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For further details about Postgraduate Studies in UPC - Barcelona School of Informatics (FiB), visit the website.

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