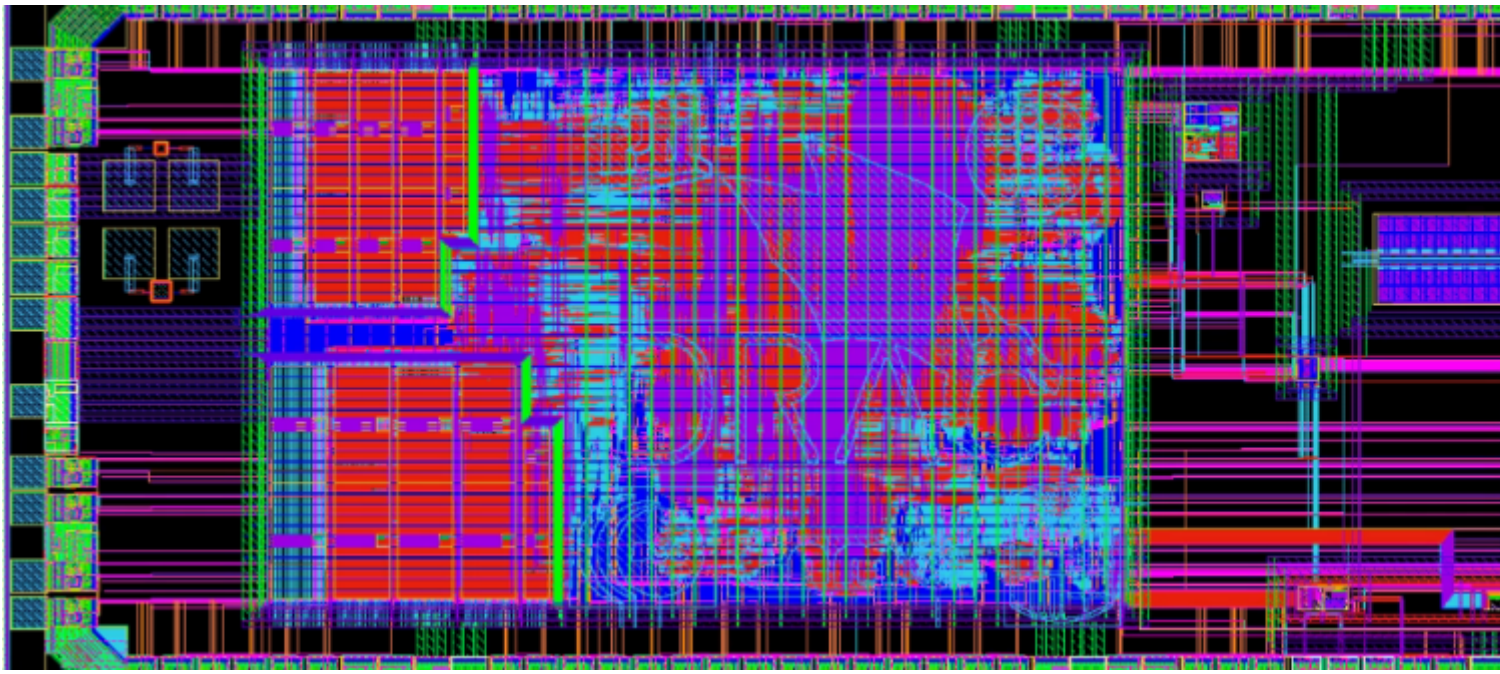
High Performance Domain-Specific Architectures



Moore’s Law is running out of steam. As a result, computer architecture plays a critical role in the design and efficient use of hardware resources. In this context, specialization and domain-specific architectures arise as a promising path to continuing to increase the performance and efficiency of computer architectures. Current heterogeneous architectures already offer a wide range of accelerators: GPUs and vector processors have been very successful exploiting data-level parallelism in many applications domains; accelerators for digital signal processing, encoding and decoding media, encryption, and networking are typical in the embedded domain; in the last years, there has been an explosion in the development of deep learning accelerators, Still, there is ample room for domain-specific acceleration in many application domains.

In the High Performance Domain-Specific Architectures team, we are developing specialized architectures for multiple application domains, ranging from traditional High Performance Computing (HPC) to emerging precision medicine and security applications. Our goal is to design novel architectures with increased performance and energy efficiency, extending the life of Moore's Law as much as possible.

Objectives

The research team is mainly focused on three different research lines:

1) Arm for HPC: The research team has collaborated with Arm and Atos in the context of the Mont-Blanc European projects, which pioneered the usage of low-power Arm processors for HPC, paving the way towards the first Arm-based supercomputers. This effort continues in the context of the Arm-BSC Centre of Excellence and the EPI project (webpage), a strategic European initiative that is developing an independent

European HPC industry based on domestic and innovative technologies.

2) Microarchitecture design and implementation: The research team is actively contributing to the Lagarto Initiative, a joint effort with multiple partners to design, verify and fabricate general purpose processors based on the RISC-V open source instruction set architecture (ISA). The first Lagarto design was fabricated in May 2019 with contributions from more than 40 researchers in five different institutions. New generations of the Lagarto processor are under active development by the research team and its collaborators (DRAC project webpage).

3) Domain-specific acceleration: The research team is accelerating precision medicine and security applications exploiting heterogeneous architectures based on CPUs, GPUs and FPGAs. Moreover, custom accelerators for these application domains are under development in the context of multiple academic and industry projects.

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

---