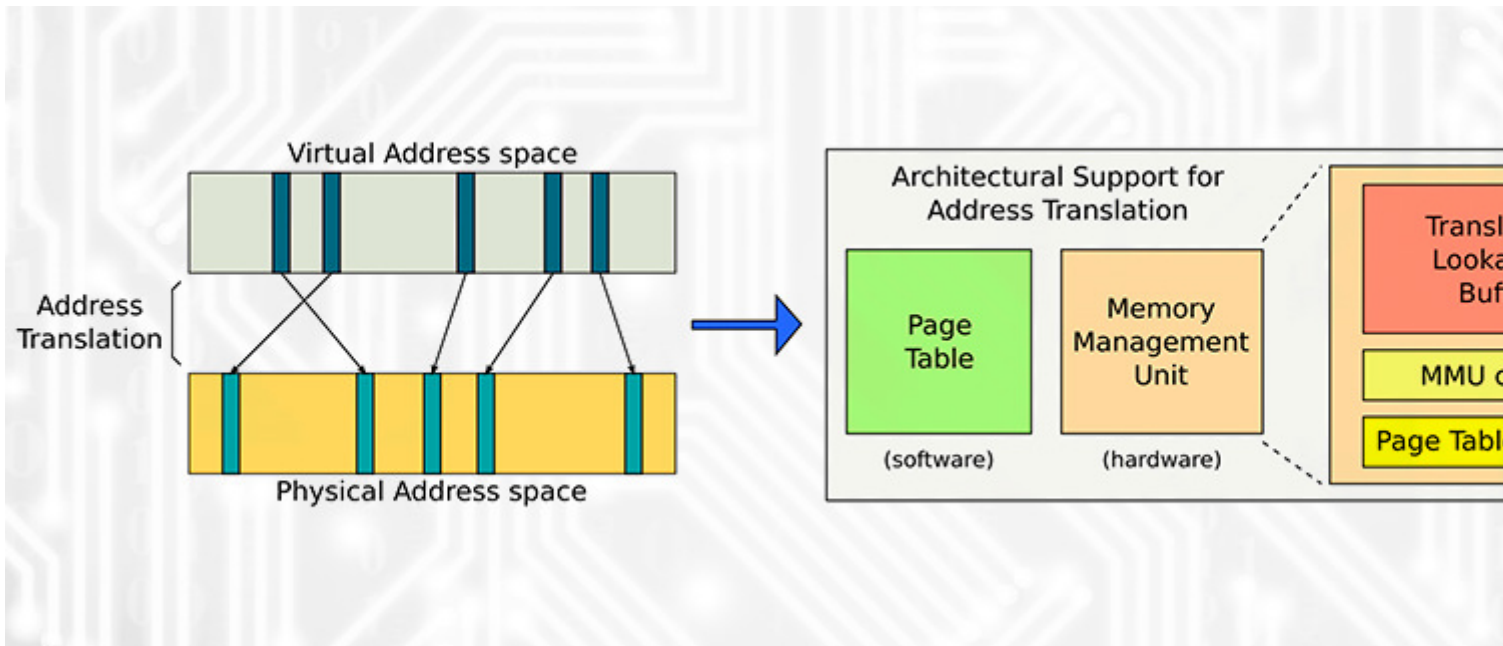


Improving Virtual Memory



Virtual memory provides many important benefits by introducing an indirection level between the virtual address space that the process sees and the physical memory that the operating system manages. However, virtual memory introduces high overheads that we seek to reduce in this project.

Summary

Virtual memory improves programmer productivity, enhances process security, and increases memory utilization. To provide these benefits, virtual memory requires an address translation from the virtual to the physical address space on every memory operation. Page-based implementations of virtual memory divide physical memory into fixed size pages, and use a per-process page table to map virtual pages to physical pages.

The hardware key component for accelerating the address translation is the Translation Lookaside Buffer (TLB), that holds recently used mappings from the virtual to the physical address space. However, the address translation incurs high (i) performance overheads due to costly page table walks after TLB misses, and (ii) energy overheads due to frequent TLB lookups on every memory operation. Our goal is to quantify these overheads and to propose hardware/software co-designs to mitigate them.

Objectives

1. Quantify the performance and energy overheads of virtual memory
2. Improve the performance of virtual memory by reducing the number of TLB misses
3. Improve the energy-efficiency of virtual memory by reducing the energy cost of TLB lookups

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