SORS: "Turquoise - 12nm 32-core RISC-V chip with a coherent mesh fabric for datacenter applications"

Abstract

In this talk, we will present Turquoise, a 64-bit 32-core Out-Of-Order RISC-V CPU chip with three levels of caches designed for datacenter applications supporting the RVA23 profile. Turquoise is fabbed with the TSMC 12nm process technology with a frequency of 2.0 GHz without overdrive. The die size is ~400 mm^2. The custom designed RISC-V core has a 512-bit vector engine supporting the full RISC-V vector extension 1.0. The core also has the latest RISC-V advance interrupt standard (AIA) and H-mode implementation to run the Xen virtualization software. Turquoise will be available with a server system board design in the E-ATX form factor. We will share our experience in architecture and silicon implementations along with our future designs of RISC-V chips.

Short Bio

Prof. Zhangxi Tan is a member of technical steering committee at RISC-V International, an adjunct professor at the Shenzhen International Graduate School?SIGS) of Tsinghua University, and a Co-Director of the RISC-V International Open-Source Laboratory (RIOS Lab). At RIOS, Prof. Tan is leading open-source hardware IP and software development that helps the RISC-V ecosystem world-class. He received his PhD in computer science from UC Berkeley in 2013 supervised by Prof. David Patterson, who is a winner of the 2017 Turing Award. Dr. Tan joined early development of RISC-V at Berkeley. His primary research is computer architecture and networks, microprocessor and VLSI designs, open-source RISC-V technologies and ecosystems, OpenEDA and PDK, non-volatile memory systems, SW/HW co-design and implementation of computer systems.

Prof. Tan is also a successful serial entrepreneur in the Silicon Valley. He was a founding engineer of Pure Storage (NYSE:PSTG), founder of OURS Technology (aquired by Aurora, NASDAQ:AUR). Prof. Tan holds more than 30 US patents in microprocessor designs, flash storage systems and hardware accelerators.

Speakers

Speaker: Prof. Zhangxi Tan. Member of technical steering committee at RISC-V International. Adjunct professor at the Shenzhen International Graduate School (SIGS) of Tsinghua University. Co-Director of the RISC-V International Open-Source Laboratory (RIOS Lab).
Host: Miquel Moretó. High Performance Domain-Specific Architectures - Group Manager. Computer Sciences, BSC.
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