SORS: Integrating posit arithmetic into a RISC-V core

Objectives

Abstract: The Posit representation, an alternative to the widely used IEEE 754 floating-point standard, offers promising benefits in terms of accuracy and execution efficiency. Nonetheless, posits are still under development, and a core that can run application-level software is needed to study the performance of this novel arithmetic format.

In this work, we introduce PERCIVAL, an application-level posit RISC-V core based on CVA6, which enables native execution of all posit instructions, including quire fused operations. Unlike previous efforts, PERCIVAL overcomes the limitations of partial posit support or software emulation, achieving full hardware integration of the complete posit instruction set. To enhance the adoption of posit representation and facilitate its usage in software development, we have incorporated a RISC-V extension for posit instructions into LLVM. FPGA and ASIC syntheses demonstrate the hardware cost of 32-bit posits, emphasizing the overhead of a quire accumulator. However, our evaluation shows significant accuracy improvements in dot products and general matrix multiplications, reducing accuracy errors by up to four orders of magnitude. Remarkably, these accuracy benefits come with no compromise in execution speed, with posits performing as fast as single-precision floats and even outperforming double-precision floats in timing.

received a BSc Degree in Computer Science and a BSc Degree in Mathematics in 2019 from the Complutense University of Madrid (UCM), where he also received his MSc Degree in Computer Science in 2021. Since 2022, he is a Teaching Assistant of Computer Science with the Department of Computer Computer Architecture and Automation at UCM. Currently, he is pursuing a Ph.D. in Computer Engineering at UCM. He has performed research stays at Politecnico di Milano, Milan. His main research areas include computer arithmetic, computer architecture, approximate computing, and deep neural networks.

Speakers

Speaker: Raúl Murillo, is pursuing a Ph.D. in Computer Engineering at UCM
Host: Miquel Moretó, High Performance Domain-Specific Architectures Associated Researcher, CS, BSC

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

---