SORS: Dromajo, Verifying RISC-V Cores

Objectives

Abstract: Processor verification engineers must find bugs before fabrication. Dromajo, a cutting-edge processor verification framework for RISC-V cores, answers this need. Dromajo started as a class project, it became the cosimulation infrastructure for out-of-order cores at Esperanto and has been adopted in multiple designs like BOOM and BlackParrot. Dromajo was designed explicitly for co-simulation of RV64GC cores. It responds to external stimuli like interrupts and debug requests and integrates seamlessly into existing testbench infrastructures.

The simulator has been augmented with a fuzzing engine to expedite the detection of bugs, thereby improving its effectiveness. Additionally, the talk will cover ongoing efforts to facilitate co-simulation of multi-core processor configurations.

Short Bio: Jose Renau is a Computer Science and Engineering Professor at the University of California, Santa Cruz. His research focuses on computer architecture, emphasizing productive hardware design flows, out-of-order cores, and RISC-V verification. His work includes developing tools like the Live Hardware Design Flow (LiveHD), architectural simulators

like ESESC, new hardware description languages like Pyrope, new design methodologies like Fluid Pipelines, and RISC-V verification tools like Dromajo.

Previous research involved Thread Level Speculation, infrared thermal measurements, power modeling, and design effort metrics/models. He holds a Ph.D. in Computer Science from the University of Illinois at Urbana-Champaign. Currently, he serves as the Chair of the IEEE TCMM and the CSE Department. For more information about his work, visit his webpage at http://www.soe.ucsc.edu/~renau.

Speakers

Speaker: Jose Renau, Computer Science and Engineering Professor at the University of California, Santa Cruz

Host: Oscar Palomar, Established Researcher, Computer Sciences - Validation, BSC

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