SORS: Democratizing high-performance microprocessor design with RISC-V and OpenEDA

Objectives

Register here for lunch following the talk (registration deadline May 31st)

Abstract: Founded in 2019 as part of Tsinghua-Berkeley Shenzhen Institute (TBSI), the RISC-V International Open Source Laboratory (RIOS Lab) began its journey of bringing the research effort of RISC-V CPU with its software and hardware ecosystems from UC Berkeley to the rest of the world. At RIOS, we have been developing out-of-order Rio series RISC-V processors targeting datacenter applications. The PicoRio series processors are industry quality designs that scale up to the 128-core configuration with a coherent-mesh support. Collaborating with RIOS industry members, we taped out PicoRio based commercial designs in several processes at different foundries. The GreenRio series processors on the other hand utilizing a complete open-source EDA and manufacturing flow. We taped out GreenRio 1.0 with the Google/Skywater 130nm OpenMPW program. It has been by far the most feature complete processor design in the OpenEDA/PDK ecosystem. The GreenRio 2.0 design won the first place in IEEE SSCS Code-a-Chip design contest in 2022 presenting at this year's ISSCC conference. Our goal is to improve the design space exploration with hardware and EDA co-design using a complete open-source flow. Using the open-source EDA on a complete open ISA, we recently conduct research on using AI to improve the PPA of our Rio series processor designs. In this talk, we will introduce our work on hardware/software co-design methodologies and iteration flows on our Rio series RISC-V processors.

Short Bio: Dr. Zhangxi Tan is an adjunct professor of Tsinghua-Berkeley Shenzhen Institute (TBSI). Dr. Tan is currently the founder and president of RiVAI Technologies Co. LTD commercializing RISC-V in datacenter applications. Dr. Tan received his PhD in computer science from UC Berkeley. Along with his advisor Prof Patterson, 2017 Turing award winner and the inventor of RISC, Dr. Tan co-direct the RISC-V international open-source laboratory (RIOS) at TBSI. Dr. Tan is specialized in computer architecture and VLSI designs. After graduating from Berkeley in 2013, he joined Pure Storage (NYSE: PSTG, a startup then) as a Founding Engineer for Pure's award winning FlashBladeTM product. After Pure, Dr. Tan founded OURS Technology (acquired by Aurora Innovation, NASDAQ:AUR) in Silicon Valley working on self-driving solid-state LiDAR sensors and vector DSPs. Dr. Tan has worked on RISC-V since his PhD work at Berkeley. Dr. Tan holds more than 30 US patents in flash storage systems, microprocessor designs and hardware accelerators. He also current serves as a member of the technical steering committee at RISC-V International. Dr. Tan's team has led numerous open-source efforts in the RISC-V community, such as RVV certification test and formal functional models, RVV GCC auto-vectorization, and etc.

Speakers

Speaker: Dr. Zhangxi Tan is an adjunct professor of Tsinghua-Berkeley Shenzhen Institute (TBSI)
Host: John Davis, LOCA director and EEA group leader, CS, BSC

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

---