LOCA SERIES/HPC@BSC: Inter-departmental collaboration as a key of success

Objectives

Download the presentation slides here and the recorded session here

Abstract:The Laboratory of Open Computer Architecture (LOCA) at Barcelona Supercomputing Center aims to break through traditional disciplinary silos and lead the research and development of European open software and hardware stacks based on the RISC-V Instruction Set Architecture for Exascale and beyond. This will be done with BSC's scientific departments to produce highly optimized grand challenge scientific applications in climate modelling, personalized medicine and energy. LOCA spans topics ranging from Computer Architecture to System Software to Applications, in both traditional HPC and emerging High-Performance Data Analytics (HPDA) and is working towards EU autonomy in HPC technologies. BSC is looking for one domain expert for each of the centre's application departments (Earth Science, Life Science and Engineering Sciences) to contribute to this aim.

This is being done with the support of BSC's Severo Ochoa award for the 2023-26 period, which aims to boost BSC capacities to codesign hardware and software, maximise internal and external synergies, expand international leadership, provide best-practice career development with strong gender actions, and enhance societal engagement and technology transfer. (https://www.bsc.es/discover-bsc/research-excellence/severo-ochoa)

Speaker: Teresa Cervero (teresa.cervero@bsc.es)

Short bio: Teresa Cervero received her Bachelor in Telecommunication Engineering, and later her PhD degree from Universidad de Las Palmas de Gran Canaria (ULPGC), in 2007 and 2013 respectively. She joined BSC in 2020, as hardware coordinator of the MareNostrum Experimental Exascale Platform (MEEP) project, and since July 2023 she is leading the Laboratory for Open Computer Architecture (LOCA) initiatives within the framework of the Severo Ochoa Programme. Her research interests include coarse-grain reconfigurable architectures, RISC-V based accelerators for HPC, FPGA-based emulation, and application-architecture co-design.

Speakers

Speaker: Teresa Cervero. Leading Research Engineer, European Exascale Accelerator - Computer Sciences, BSC