LOCA SERIES: "Enabling high-level parallel programming on multi-FPGA clusters"

Abstract:

Field Programmable Gate Arrays (FPGA) are still relatively new in the High Performance Computing (HPC) field. Hence, they still lack a mature ecosystem that allows non-FPGA experts to scale an application with many devices operating in parallel. In this presentation, I will talk about how we added support for message passing inspired by the Message Passing Interface (MPI) to the Marenostrum Exascale Emulation Platform (MEEP) cluster.
I will introduce the OmpSs@FPGA programming model, which allows C/C++ code to run on the FPGA and call functions that behave like the well-known MPI_Send/Recv. I will also give details about how to implement the message passing runtime over the MEEP 100Gb Ethernet network, as well as the challenges I found during development. On the software side, I will show how to manage FPGAs that are PCIe-hosted by remote CPU nodes. I.e. from any CPU node we can load the bitstream, configure it, and transfer data to FPGAs that are attached to a different node. Finally, I will present the evaluation results in the MEEP cluster: Bandwidth of FPGA-FPGA, and CPU-FPGA local and remote communication, as well as the performance of benchmarks scaling from 1 to 64 FPGAs. The benchmarks are N-body, Heat with Gauss-Seidel solver and Cholesky decomposition. Comparing the results with the MareNostrum 4 supercomputer, we get 2.3x and 3.5x better performance per power for N-body and Heat.

Speaker: Juan Miguel de Haro Ruiz.

Short bio:
Juan Miguel de Haro Ruiz received the BS degree in informatics engineering and the MS degree specialized in high performance computing from Universitat Politècnica de Catalunya (UPC) in 2018 and 2020. He is currently working towards the PhD degree with the Computer Architecture Department, UPC. He is also with the OmpSs@FPGA Team, Programming Models Group at the BSC. His research interests include parallel and reconfigurable architectures, hardware acceleration, and runtime systems for heterogeneous and distributed architectures.

Speakers

Speaker: Juan Miguel de Haro Ruiz. Research Engineer OmpSs@FPGA Team, Programming Models Group at the BSC.
Host: Xavier Martorell. Parallel Programming Models Group Manager, Computer Sciences, BSC.
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