Hybrid BSC RS: Chiplets and EDA: Reimagining the Journey Ahead

Objectives

Abstract: Advances in modern manufacturing and integration technologies have enabled rapid progress in advanced packaging in the past decade, ushering in a new era of SysMoore designs characterized by higher density and increased performance and data bandwidth. The next decade promises to be the time for the design automation (EDA) industry to give wings to engineering teams across the industry – foundry, OSAT, chip and 3D IC system designers of the SysMoore era, to accelerate the technological and scalability gains and drive the next wave of transformative products.
Ensuring time-zero manufacturing quality, high yield and life-time reliability and safety of designs is key to realizing these next-generation of innovative products powering trillions of connecting devices of future. This requires comprehensive design verification solutions for the system-of-chips and chiplets, coupled with holistic design and manufacturing enablement methodology. In this talk, we will provide insights into some of the myriad manufacturing, quality and productivity challenges faced by 3DIC design teams; and discuss the state of the art in die-to-die IP and end-to-end design automation to address them. We will discuss how innovations in 3D design-for-test/manufacturing/reliability (DFx), silicon-lifecycle-management (SLM) and yield analysis are paving the way for higher quality and more productive SysMoore era heterogenous integration and disaggregation designs.

Short Bio: Dr. Ming Zhang is a Distinguished Architect at Synopsys, driving long-term technology strategy and market development for the Electronic Design Automation Group. He led corporate strategy for 3DIC technology upon joining Synopsys in 2021. Prior to Synopsys, he was a circuit designer at Intel specializing in low-power and fault-tolerant designs, foundry engineer at Samsung specializing in DFX, software developer at AI startups working on algorithm development and cloud deployment, and, most recently, the co-founder and CEO of a Silicon Valley chiplet startup, zGlue. Dr. Zhang holds a Ph.D. EE in VLSI from the University of Illinois at Urbana-Champaign (UIUC), an M.S. in MEMS from UIUC, and a B.S. in Physics from Peking University in China.

Speakers

Speaker: Dr. Ming Zhang, Distinguished Architect at Synopsys
Host: Miquel Moretó, High Performance Domain-Specific Architectures Associated Researcher, Computer Sciences