

## Leveraging Hardware QoS to Control Contention in the Xilinx Zynq UltraScale+ MPSoC

**URL:** <https://drops.dagstuhl.de/opus/volltexte/2021/13934/>

**Authors:** [Serrano-Cases, Alejandro](#) / [Reina, Juan](#) / [Abella, Jaume](#) / [Mezzetti, Enrico](#) / [Cazorla, Francisco](#)

**Research Lines:** [COTS multicore real-time systems](#)

**Publication:** 33rd Euromicro Conference on Real-Time Systems (ECRTS 2021)

**Place Published:** Schloss Dagstuhl - Leibniz-Zentrum für Informatik

**Paraules clau:** [quality of service](#), [Real-time systems](#), [MPSoC](#), [Multicore Contention](#), [Computer systems organization ? Real-time system architecture](#)

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

---

**Source URL (retrieved on 21 oct 2024 - 00:31):** <https://www.bsc.es/ca/research-and-development/publications/leveraging-hardware-qos-control-contention-the-xilinx-zynq>