

## [Another Trip to the Wall: How Much Will Stacked DRAM Benefit HPC?](#)

**URL:** <http://dl.acm.org/citation.cfm?id=2818955>

**Authors:** [Radulovic, Milan](#) / [Zivanovic, Darko](#) / [Ruiz, Daniel](#) / [de Supinski, Bronis](#) / [McKee, Sally](#) / [Radojkovic, Petar](#) / [Ayguade, Eduard](#)

**Research Lines:** [Memory systems for HPC](#)

**Publication:** Proceedings of the International Symposium on Memory Systems (MEMSYS '15)

**Place Published:** Washington DC, DC, USA

**Pagination:** 31-36

**Paraules clau:** [Bandwidth](#), [DRAM](#), [high bandwidth memory \(HBM\)](#), [HPC](#), [hybrid memory cube \(HMC\)](#), [latency](#), [Memory wall](#)

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

---

**Source URL (retrieved on 18 jul 2024 - 21:24):** <https://www.bsc.es/ca/research-and-development/publications/another-trip-the-wall-how-much-will-stacked-dram-benefit-hpc>