

STT-MRAM: STT-MRAM Main Memory for High Performance Computing Clusters

Description

High performance computing (HPC) is recognized as a driving force for innovation in science and technology. HPC clusters are indispensable tools for research, development, and analysis in many fields of science and engineering. HPC is a global market funded by industry, financial institutions, governments, defense, and academia, with high revenues that are expected to grow in the following years. In state-of-the-art HPC clusters, memory system is one of the most important design issues that significantly affects system performance. Memory systems became significant contributors to the overall system power requirements, energy consumption, and the operational cost of large HPC systems. Since it is questionable whether conventionally-used memory architectures based on mature DRAM technology aims to meet the needs of next-generation HPC systems, significant effort is invested in research and development of novel memory technologies.

In this project, Barcelona Supercomputing Center explored whether spin-transfer torque magnetic random access memory (STT-MRAM) is a good candidate for main memory systems in next-generation HPC clusters. We analyzed performance and energy consumption of multi-threaded HPC applications running on large-scale clusters with STT-MRAM main memory, and to compare the results with conventional DRAM memory systems. Moreover, we determined which parts of the memory architecture and organization should be enhanced to properly exploit the features of the STT-MRAM technology. We incorporated these architectural changes into a system simulator, and evaluated their impact on system performance and energy efficiency.

Barcelona Supercomputing Center considered the project as the first step toward using next-generation STT-MRAM memory systems for high-performance and energy-efficient supercomputing. The improvements in the memory systems can directly translate to higher performance and lower operational cost in large HPC systems. Also, we expect that dissemination of our work will motivate follow-up studies that will explore the suitability of STT-MRAM for memory systems in other domains.

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