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Description

The growing need to transfer massive amounts of data among multitudes of interconnected devices for e.g., self-driving vehicles, IoT industry 4.0 has led to a quest towards low-power and secure approaches to locally processing data. Neuromorphic computing, a brain-inspired approach, addresses this need by radically changing the processing of information. Although neuromorphic electrical computing systems offer advantages in terms of CMOS implementations and scalability, they inherit limitations of conventional electronics such as low energy-efficiency, high latency and low bandwidth density. Besides, such systems often require robust security layers for e.g., safety-critical applications.

Security layers based on memory-stored secret keys are prone to several types of memory-accessing attacks. Therefore, silicon hardware approaches for security primitives such as physical unclonable functions (PUFs) are currently investigated because of their absence of long-term digital memory storage. Although electronic PUFs have received major attention thanks to their native CMOS implementation, for secure authentication they are prone to machine learning and side-channel attacks due to their CMOS technology.

The NEUROPULS project aims to build next-generation low-power and secure edge-computing systems by developing novel photonic computing architectures and security layers based on photonic PUFs in augmented silicon photonics CMOS-compatible platforms. The integration of emerging non-volatile phase change materials for synapses/neurons and III-V materials for on-chip spiking sources, for the first time, will allow to build novel neuromorphic accelerators featuring RISC-V compliant interfaces for smooth adoption and programmability. Optimal performance will be achieved thanks to a novel full-system simulation platform for design space exploration. Three relevant use-cases will be considered for benchmarking to demonstrate 2 orders of magnitude energy efficiency improvement.

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Source URL (retrieved on 11 ago 2024 - 13:17): <https://www.bsc.es/ca/research-and-development/projects/neuropuls-neuromorphic-energy-efficient-secure-accelerators-based>