

EPI SGA1: Specific Grant Agreement 1 of the European Processor Initiative (EPI)

Description

The EPI SGA1 project will be the first phase of the European Processor Initiative FPA, whose aim is to design and implement a roadmap for a new family of low-power European processors for extreme scale computing, high-performance Big-Data and a range of emerging applications. EPI SGA1 will:

- Develop the roadmap for the full length of the EPI initiative
- Develop the first generation of technologies through a co-design approach (IPs for general-purpose HPC processors, for accelerators, for trusted chips, software stacks and boards)
- Tape-out of the first generation chip by integrating the IPs developed
- Validate this chip in the HPC context and in the automotive context using a demonstration platform.

The project will deliver a high performance, low power processor, implementing vector instructions and specific accelerators with high bandwidth memory access. The EPI processor will also meet high security and safety requirements. This will be achieved through intensive use of simulation, development of a complete software stack and tape-out in the most advanced semiconductor process node. SGA1 will provide a competitive chip that can effectively address the requirements of the HPC, AI, automotive and trusted IT infrastructure markets. scientific and industrial users on the other. The consortium covers the complete range of expertise, skills and competencies needed to design and execute a sustainable roadmap for research and innovation in HPC and emerging applications, including Big Data, which will bring results right to market. In order to have a solution for 2022-23, EPI will design and develop the first European ARM-based HPC System on Chip, which will combine ARM cores with European technology.

In parallel, the consortium will design and develop an accelerator based on the RISC-V instruction set architecture, containing only European and Open-Source technology. This technology is not as mature but has a lot of potential in the medium to long term. Both elements will be implemented and validated in a prototype. Subsequent generations of them will form the basis for future heterogeneous exascale systems.

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