DESCARTES: Dynamic Extensible Vector Architectures and Systems

Description

The world has entered the era of ubiquitous High Performance Computing (HPC), where massive data sets and their associated computation impact all facets of modern life. However, while new software frameworks enable very high programmer productivity, ironically, all of the rich semantics from the algorithms are stripped away when applications run on the hardware, forcing computer architects to implement expensive and often inefficient hardware components to reconstruct the lost programme information.

The goal of the DESCARTES project is to maintain high the programmer productivity and dramatically improve system efficiency and performance by defining dynamic, extensible vector architectures and systems for both traditional HPC and emerging High Performance Data Analytics (HPDA) workloads leveraging malleable hardware.

DESCARTES will develop new vector computer architectures, which will allow hardware to exploit semantics for a broad set of applications. This will be achieved by propagating semantic information from application to architecture and then rightsizing as well as retuning the DESCARTES hardware to match application needs. This will result in dynamic software/hardware co-optimization for future HPC and HPDA systems, going beyond current co-design approaches.

DESCARTES will revolutionize the way HPC architectures are designed by proposing a new malleable vector architecture; DESCARTES results will break the chains that prevent the optimal use of computer architectures and will dramatically improve system performance and energy efficiency when executing HPC and HPDA workloads.

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