De-RISC: De-RISC: Dependable Real-time Infrastructure for Safety-critical Computer

Description

The De-RISC project addresses computer systems within the space and aviation domains. De-RISC Dependable Real-time Infrastructure for Safety-critical Computer is a proposed project where an international consortium will introduce a hardware and software platform based aroundthe RISC-V ISA. The work proposed in this project is to productize a multi-core RISC-V system-on-chip design already owned by CG and to portthe XtratuM hypervisor owned by FEN to that design to create a full platform consisting of hardware and software for future European developments within space and aeronautical applications.De-RISC brings critical features to the market that make it unique in front of the competition:

1. No US export restrictions: most existing products use US technology, thus subject to US export control. De-RISC s IP core platform andsoftware will not be subject to any US regulatory influence by building on RISC-V.
2. Multi-core interference mitigation concepts by BSC integrated in the RISC-V SoC and validated by TRT become a unique feature, and will provide a key advantage w.r.t. competitors by limiting drastically interference while preserving high-performance operation.
3. Portability: The proposed development will create a RISC-V HW/SW platform that can be implemented in FPGAs and application specificstandard products. This provides an edge for integrators that can adapt their choice of implementation technology based on mission requirements.
4. Fault-tolerance concepts: The platform will be provided by companies with experience in the space domain and with heritage in design of faulttolerantsystems.
5. Future-proof selection for new platforms: New software products are not being ported to SPARC and PowerPC architectures.

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