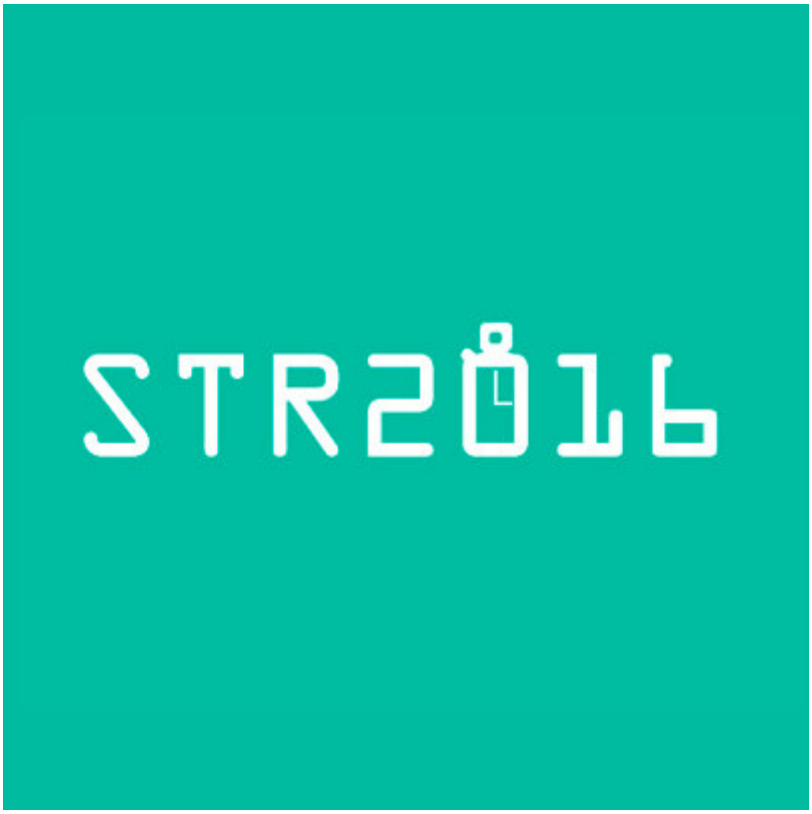
Francisco J. Cazorla, keynote speaker at the Spanish Conference of Computer Science



The BSC researcher Francisco J. Cazorla will be a keynote speaker at the V Simposio de Sistemas de Tiempo Real (STR 2016) as part of the Spanish Conference of Computer Science (CEDI) that is taking place in Salamanca today.

STR is the premier real-time systems conference in Spain. Dr. Cazorla will discuss the use of high-performance computer architectures in embedded systems such as those found in aeroplanes, trains and cars. This is an area in which Dr. Cazorla and the BSC's CAOS group have been very active in recent years as in both European projects such as PROXIMA, P-Socrates or Safure and bilateral projects, including those with the European Space Agency and German-based company DENSO among others.

You can see the programme here.

Further information about Cazorla's presentation is below:

Title: Time Predictability and Composability in High-Performance Mixed-Criticality Multicore Systems

Abstract: The fundamental paradigms for the definition of Critical-Real Time Embedded Systems (CRTES) architectures are changing due to cost pressure, flexibility, extensibility and the demand for increased functional complexity. CRTES have been based on the federated architecture paradigm, which simplify

verification by providing a separation of responsibilities, hence enabling each provider to implement the hardware and the software for a particular function independently from other suppliers. However, implementing an increasing amount of functionality on a Federated Architecture requires a high number of hardware units, making federated implementations inefficient in terms of size, weight and power consumption.

To cope with such a problem, the automotive and avionics industries are adopting Integrated Architectures. (IA). One fundamental requirement of integrated architectures is to ensure that incremental qualification (verification) is possible, whereby each software partition can be subject to verification and validation – including timing analysis – in isolation, independent of the other partitions, with obvious benefits for cost, time and effort.

In this talk I will focus on the timing component of incremental qualification. I will present some hardware support that can enable composability while providing high performance. I will also talk about about existing software support to increase time predictability and time composability. I will also talk about the feasibility of a probabilistic timing analysis approach, and the hardware support required in order to enable it, as a way to provide high performance and time composability.

Biography: Francisco J. Cazorla is a researcher at the National Spanish Research Council (CSIC). He is currently the leader of the group on Interaction between the Operating System and the Computer Architecture at Barcelona Supercomputing Centre (www.bsc.es/caos). His research area focuses on multithreaded architectures for both high-performance and real-time systems. He has co-authored over 100 papers in international refereed conferences. He has participated in several projects with industry including several processor vendor companies (IBM, Sun microsystems) and European FP6 (SARC) and FP7 Projects (MERASA, parMERASA, SAFURE, PROARTIS). He currently leads the PROXIMA project and one project with the European Space Agency. In 2011, he was awarded by the Massachusetts Institute of Technology (MIT) as one of the 10 most promising innovators in Spain (under 40 years old) whose technical work has been very successful in recent years and has great potential for development for decades. In 2015, he has been distinguished with one of the 10 medals that the Spanish Royal Academy of Engineering awards to outstanding Spanish engineers under

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