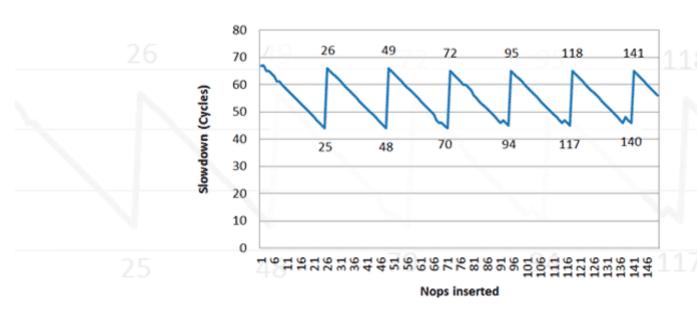


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## BSC demonstrates better performance of multi-core processors in real-time critical systems thanks to maximum latency achieved using only measurements



The <u>Barcelona Supercomputing Center</u> (BSC) has demonstrated that the arbitration policies for access to shared resources in a multi-core system have a maximum latency and that this latency can be derived from measurements alone. This eliminates the need for processor documentation, which is often either confidential or does not provide all of the necessary information.

As a result of this breakthrough, **multi-core processors** which were **not initially intended for real-time critical systems can now be used, leading to the performance of such systems being significantly higher**. This paves the way to more powerful systems with more functionalities.

Real-time critical systems need to have ways of upper bounding the worst-case execution time in processors that were not originally planned to be part of such systems. That's to say, we need to be able to **ensure the reliability of the timing guarantees on multi-core processors**.

Real-time critical systems are used in many sectors. In medicine, they are used in telecommunications in devices that have to provide a quick response at an exact moment, such as insulin pumps. They are also used in the aviation and automotive industries to produce safer and more efficient aircraft and cars.

For BSC Computer Science department researcher **Jaume Abella**, "allowing industry to incorporate the powerful multi-core processors that are on the market at affordable prices into their critical systems means that improved performance of these systems can be guaranteed in all operating conditions. This opens the door to any number of applications which were simply not possible without being prohibitively expensive. Thanks to this technology, we will soon see self-driving cars for sale for €10,000 or €100 mobile phones able to monitor pacemakers."

Abella goes on to explain that "we have shown that for FIFO (first-in first-out) policies with maximum

contention (in which the other cores are using the shared resources at 100%), where the number of cores in the multi-core processor is N and the service time of the shared resources is L, the latency due to contention varies between (N-2) x L and (N-1) x L. In the case of a round-robin policy, we've shown that it varies between 0 and (N-1) x L. These results have been obtained from measurements and the methodology has been assessed with the specification of the particular processor studied."

These results have come out of the <u>SAFURE research project</u>, in which BSC is a partner. The project targets the design of cyber-physical systems by implementing a methodology that ensures safety and security "by construction". The current approach for security on safety-critical embedded systems is generally to keep sub-systems separated, but this approach is now being challenged by technological evolution towards openness, increased communications and use of multi-core architectures.

The SAFURE project consortium is made up of 12 research centres and companies. It started in February 2015 and will run until January 2018. It has received over €5 million from the European Union's Horizon 2020 programme.

(Fig: performance measured in a multi-core prototype for spatial systems)

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Barcelona Supercomputing Center - Centro Nacional de Supercomputación

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