966_24_CS_V_RE2-3

Job Reference

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Position

Verification engineer for core level - DARE (RE2-3)

Data de tancament

Dissabte, 15 Febrer, 2025
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About BSC

The Barcelona Supercomputing Center - Centro Nacional de Supercomputación (BSC-CNS) is the leading supercomputing center in Spain. It houses MareNostrum, one of the most powerful supercomputers in Europe, was a founding and hosting member of the former European HPC infrastructure PRACE (Partnership for Advanced Computing in Europe), and is now hosting entity for EuroHPC JU, the Joint Undertaking that leads large-scale investments and HPC provision in Europe. The mission of BSC is to research, develop and manage information technologies in order to facilitate scientific progress. BSC combines HPC service provision and R&D into both computer and computational science (life, earth and engineering sciences) under one roof, and currently has over 1000 staff from 60 countries.

Look at the BSC experience:
BSC-CNS YouTube Channel
Let's stay connected with BSC Folks!

We are particularly interested for this role in the strengths and lived experiences of women and underrepresented groups to help us avoid perpetuating biases and oversights in science and IT research. In instances of equal merit, the incorporation of the under-represented sex will be favoured.

We promote Equity, Diversity and Inclusion, fostering an environment where each and every one of us is appreciated for who we are, regardless of our differences.

If you consider that you do not meet all the requirements, we encourage you to continue applying for the job offer. We value diversity of experiences and skills, and you could bring unique perspectives to our team.

Context And Mission

DARE European Supercomputing Project.

BSC is looking for talented and motivated professionals with expertise in Design Verification for a chip integrating an European HPC accelerator in the context of the DARE Project and other related research projects. The design is based on RISC-V architecture. BSC contributes a RISC-V vector accelerator to the EPI project and verifying the functional correctness of the chip is key for success.

Key Duties

- You will use your design and verification expertise to verify complex RISC-V digital designs, focused on scalar processors that will support vector instructions via a vector accelerator and connected to memory hierarchy using AMBA CHI.
- You will collaborate closely with design and verification engineers in active projects and perform hands-on verification, and contribute to design, build, and integrate the designs.
- Using your UVM, SystemVerilog and problem-solving skills, you will build efficient and effective verification environments that exercise processor designs through their corner-cases and expose all types of bugs.
- You will be responsible for the full life cycle of verification, including verification planning, test and assertion implementation, failure triaging, debugging, coverage definition and others.
- You will automatize the processes by creating and maintaining verification & post-processing scripts for verification, triaging, coverage and debugging.
- You will train others in the configuration, deployment, use and/or maintenance of verification software, scripts and workflows.
- You supervise, guide and coordinate the work of less experienced Verification engineers working in the project.
- You will define and implement coverage plans for the design, and analyse the code and functional coverage results obtained to identify verification holes and to show progress towards tape-out.

Requirements

- Education
    - BS degree in Electrical Engineering, Computer Engineering, or equivalent, with demonstrable professional experience.

- Essential Knowledge and Professional Experience

- Experience with the full verification life cycle from test planning to sign-off.
- Working knowledge of Universal Verification Methodology(UVM), writing test plans, simulating, debugging, and documenting results
- Knowledge of and experience with industry-standard simulators (Model/QuestaSim, VCS, etc.), revision control systems and regression systems.
- Experience in the following key DV methodologies: UVM, cosimulation, SystemVerilog Assertions, functional coverage, Assembly/C-based random/constrained-random Verification, Verification IPs.
- Experienced in developing a DV plan based on Functional Specification, create and build the necessary verification test bench/infrastructure, develop tests and verify the design.
- Experience in the creation and implementation of verification plans of complex digital design blocks by fully understanding the design specification and interacting with design engineers to identify important verification scenarios.
- Experience defining and implementing functional coverage, working with cross functional teams (DV/Arch/Design).
- Strong debugging and triaging skills and ability to work with design engineers to deliver functionally correct design blocks, execute tests, analyze data, and prepare reports summarizing results and statistics.
- Strong scripting experience using scripting languages like Python, Perl, Bash or Tcl to perform support adjustments and customization of design and verification flows. Familiarity with Linux.
- Experience in the implementation of SystemVerilog UVM testbenches for a complex digital design, coupling with a reference model for co-simulation.
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- Experience in the analysing of coverage reports and improving results to reach closure.
- Excellent interpersonal, written, and verbal communication skills.
- Ability to work as part of a cross-functional team according to an established timeline
- Deep understanding of Modern in-order and out-of-order processor core and accelerator designs.
- Experience with one or more Instruction Set Architectures (ISAs) including RISC-V, and their implementation within in-order and out-of-order processor cores.

- Additional Knowledge and Professional Experience
  - Experience with verification of top-level and processor-based SoC and DLP acceleration (GPU/SIMD/Vector) is a big plus.
  - Good knowledge of common protocols and interfaces such as AXI, SPI, JTAG or UART.
  - Good knowledge of AMBA CHI
  - Fluency in English is essential, Spanish is welcome.

- Competences
  - The candidate must be an effective communicator, multitask, and work well on collaborative designs.
  - Keeps abreast of technology trends.
  - Ability to think creatively.
  - Ability to work independently and make decisions.
  - Ability to take initiative, prioritize and work under set deadlines.

Conditions

- The position will be located at BSC within the Computer Sciences Department
- We offer a full-time contract (37.5h/week), a good working environment, a highly stimulating environment with state-of-the-art infrastructure, flexible working hours, extensive training plan, restaurant tickets, private health insurance, support to the relocation procedures
- Duration: Open-ended contract due to technical and scientific activities linked to the project and budget duration
- Holidays: 23 paid vacation days plus 24th and 31st of December per our collective agreement
- Salary: we offer a competitive salary commensurate with the qualifications and experience of the candidate and according to the cost of living in Barcelona
- Starting date: January 2025

Applications procedure and process

All applications must be submitted via the BSC website and contain:

- A full CV in English, including contact details.
- A cover/motivation letter with a statement of interest in English, clearly specifying for which specific area and topics the applicant wishes to be considered. Additionally, two references for further contacts must be included. Applications without this document will not be considered.

Development of the recruitment process

The selection will be carried out through a competitive examination system ("Concurso-Oposición"). The recruitment process consists of two phases:

1. **Curriculum Analysis:** Evaluation of previous experience and/or scientific history, degree, training, and other professional information relevant to the position. - ***40 points***
2. **Interview phase:** The highest-rated candidates at the curriculum level will be invited to the interview phase, conducted by the corresponding department and Human Resources. In this phase, technical competencies, knowledge, skills, and professional experience related to the position, as well as the required personal competencies, will be evaluated. - ***60 points.*** *A minimum of 30 points out of 60 must be obtained to be eligible for the position.*

The recruitment panel will be composed of at least three people, ensuring at least 25% representation of women.

In accordance with OTM-R principles, a gender-balanced recruitment panel is formed for each vacancy at the beginning of the process. After reviewing the content of the applications, the panel will begin the interviews, with at least one technical and one administrative interview. At a minimum, a personality questionnaire as well as a technical exercise will be conducted during the process.

The panel will make a final decision, and all individuals who participated in the interview phase will receive feedback with details on the acceptance or rejection of their profile.

At BSC, we seek continuous improvement in our recruitment processes. For any suggestions or comments/complaints about our recruitment processes, please contact recruitment [at] bsc [dot] es.

For more information, please follow this link.

Deadline

The vacancy will remain open until a suitable candidate has been hired. Applications will be regularly reviewed and potential candidates will be contacted.

OTM-R principles for selection processes

BSC-CNS is committed to the principles of the Code of Conduct for the Recruitment of Researchers of the European Commission and the Open, Transparent and Merit-based Recruitment principles (OTM-R). This is applied for any potential candidate in all our processes, for example by creating gender-balanced recruitment panels and recognizing career breaks etc.
BSC-CNS is an equal opportunity employer committed to diversity and inclusion. We are pleased to consider all qualified applicants for employment without regard to race, color, religion, sex, sexual orientation, gender identity, national origin, age, disability or any other basis protected by applicable state or local law.
For more information follow this link

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

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