941_24_CS_CORE_RE2

Job Reference

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Position

Research Engineer - RTL OoO Core Development - DARE (RE2)

Data de tancament

Dissabte, 15 Febrer, 2025
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About BSC

The Barcelona Supercomputing Center - Centro Nacional de Supercomputación (BSC-CNS) is the leading supercomputing center in Spain. It houses MareNostrum, one of the most powerful supercomputers in Europe, was a founding and hosting member of the former European HPC infrastructure PRACE (Partnership for Advanced Computing in Europe), and is now hosting entity for EuroHPC JU, the Joint Undertaking that leads large-scale investments and HPC provision in Europe. The mission of BSC is to research, develop and manage information technologies in order to facilitate scientific progress. BSC combines HPC service provision and R&D into both computer and computational science (life, earth and engineering sciences) under one roof, and currently has over 1000 staff from 60 countries.

Look at the BSC experience:
BSC-CNS YouTube Channel
Let's stay connected with BSC Folks!

We are particularly interested for this role in the strengths and lived experiences of women and underrepresented groups to help us avoid perpetuating biases and oversights in science and IT research. In instances of equal merit, the incorporation of the under-represented sex will be favoured.

We promote Equity, Diversity and Inclusion, fostering an environment where each and every one of us is appreciated for who we are, regardless of our differences.

If you consider that you do not meet all the requirements, we encourage you to continue applying for the job offer. We value diversity of experiences and skills, and you could bring unique perspectives to our team.

Context And Mission

DARE European Supercomputing Project

BSC has an open position for a Research Engineer in the Computer Sciences Department to be a part of an active Computer Architecture research group working on designing and developing a high-end out-of-order processor for the HPC Digital Autonomy with RISC-V in Europe project or DARE. The DARE objectives are:
- Contribute to European technological sovereignty by building a complete software/hardware ecosystem for HPC based on RISC-V, optimized for critical EU HPC applications by using a co-design approach.
- Produce a long-term roadmap with a critical timeline, milestones, and all the necessary activities needed to build and deploy post-exascale systems in Europe using European technology.
- Deliver EU-owned, energy-efficient, high-end processors and accelerators designed for industrial-grade HPC and Cloud solutions.

Key Duties

- Research of computer architectural techniques and development of RTL hardware structures related to superscalar OoO core design to improve the efficiency, scalability, and performance of a current RISC-V core.
- Review and analyze the state-of-the-art performance techniques for OoO processor architectures to identify the most effective approaches.
- Design RTL structures by implementing the selected techniques for RISC-V CPU architectures. Implement complex control logic, data paths, and microarchitectural features in SystemVerilog.
- Integration into RISC-V Core: This integration should provide an efficient and configurable means of RISC-V processor cores with the new capabilities, demonstrating a tradeoff balance with performance improvements.
- Verification and Validation: Develop a verification strategy with CoCoTB for the derived modules and Python hardware modeling. Implement verification tests and validation procedures to ensure correctness and functionality.
- Performance Evaluation: Evaluate the impact of the new capabilities on the RISC-V processor core through extensive simulation and benchmarking. Measure the improvements in terms of execution efficiency, reduced cycle count, and overall performance.
- Follow the methodology and quality standards for the code base development.
- Documentation and Reporting: Document design specifications, microarchitecture, and test plans. Prepare reports and presentations on design progress, issues, and performance metrics.
- Tool and Methodology Development: Develop and maintain scripts and tools to automate design and verification tasks. Contribute to the improvement of design and verification methodologies within the team.
- Code Quality and Maintenance: Ensure high-quality, maintainable, and reusable RTL code. Perform code reviews and provide constructive feedback to peers.
- Compliance and Standards: Ensure design compliance with industry standards and best practices. Follow project-specific guidelines and contribute to the establishment of new standards within the team.

Requirements

- Education
  - BS or MS in Telecommunication, Electronics, Computer Science, or Computer Engineering.

- Essential Knowledge and Professional Experience
  - Logic Circuit Design Knowledge.
  - Proficiency in SystemVerilog.
  - Computer architecture Knowledge.
  - Familiarity with RISC-V Specification
  - Git version control system Knowledge.
  - Python and CoCoTB.
  - Proficiency with standard open-source and industry tools for RTL simulation. Computer architecture Knowledge.
  - Direct Programming Interface for HW Modeling and Host Interfacing.
  - Make, Bash, Docker

- Additional Knowledge and Professional Experience
  - Knowledge and experience of programming (with C, C++)
  - Experience working with Linux operating system

- Competences
  - Good English Communication skills (written and speaking)
  - Teamwork and Collaboration
  - Assertive Comunication
  - Adaptability
  - Problem-Solving
  - Critical Thinking
  - Time Management
  - Interpersonal Skills
  - Attention to Detail

Conditions

- The position will be located at BSC within the Computer Sciences Department
- We offer a full-time contract (37.5h/week), a good working environment, a highly stimulating environment with state-of-the-art infrastructure, flexible working hours, extensive training plan, restaurant tickets, private health insurance, support to the relocation procedures
- Duration: Open-ended contract due to technical and scientific activities linked to the project and budget duration
- Holidays: 23 paid vacation days plus 24th and 31st of December per our collective agreement
- Salary: we offer a competitive salary commensurate with the qualifications and experience of the candidate and according to the cost of living in Barcelona
- Starting date: Month 0

Applications procedure and process

The selection will be carried out through a competitive examination system ("Concurso-Oposición"). The recruitment process consists of two phases:

1. **Curriculum Analysis:** Evaluation of previous experience and/or scientific history, degree, training, and other professional information relevant to the position. - ***40 points***
2. **Interview phase:** The highest-rated candidates at the curriculum level will be invited to the interview phase, conducted by the corresponding department and Human Resources. In this phase, technical competencies, knowledge, skills, and professional experience related to the position, as well as the required personal competencies, will be evaluated. - ***60 points.*** *A minimum of 30 points out of 60 must be obtained to be eligible for the position.*

The recruitment panel will be composed of at least three people, ensuring at least 25% representation of women.

In accordance with OTM-R principles, a gender-balanced recruitment panel is formed for each vacancy at the beginning of the process. After reviewing the content of the applications, the panel will begin the interviews, with at least one technical and one administrative interview. At a minimum, a personality questionnaire as well as a technical exercise will be conducted during the process.

The panel will make a final decision, and all individuals who participated in the interview phase will receive feedback with details on the acceptance or rejection of their profile.

At BSC, we seek continuous improvement in our recruitment processes. For any suggestions or comments/complaints about our recruitment processes, please contact recruitment [at] bsc [dot] es.

For more information, please follow this link.

Deadline

The vacancy will remain open until a suitable candidate has been hired. Applications will be regularly reviewed and potential candidates will be contacted.

OTM-R principles for selection processes

BSC-CNS is committed to the principles of the Code of Conduct for the Recruitment of Researchers of the European Commission and the Open, Transparent and Merit-based Recruitment principles (OTM-R). This is applied for any potential candidate in all our processes, for example by creating gender-balanced recruitment panels and recognizing career breaks etc.
BSC-CNS is an equal opportunity employer committed to diversity and inclusion. We are pleased to consider all qualified applicants for employment without regard to race, color, religion, sex, sexual orientation, gender identity, national origin, age, disability or any other basis protected by applicable state or local law.
For more information follow this link