441_24_CS_HWE_R1

Job Reference

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Position

HW Research Engineer- PhD position (FPGA and RISC-V) (R1)

Data de tancament

Dimecres, 31 Juliol, 2024
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About BSC

The Barcelona Supercomputing Center - Centro Nacional de Supercomputación (BSC-CNS) is the leading supercomputing center in Spain. It houses MareNostrum, one of the most powerful supercomputers in Europe, was a founding and hosting member of the former European HPC infrastructure PRACE (Partnership for Advanced Computing in Europe), and is now hosting entity for EuroHPC JU, the Joint Undertaking that leads large-scale investments and HPC provision in Europe. The mission of BSC is to research, develop and manage information technologies in order to facilitate scientific progress. BSC combines HPC service provision and R&D into both computer and computational science (life, earth and engineering sciences) under one roof, and currently has over 1000 staff from 60 countries.

Look at the BSC experience:
BSC-CNS YouTube Channel
Let's stay connected with BSC Folks!

We are particularly interested for this role in the strengths and lived experiences of women and underrepresented groups to help us avoid perpetuating biases and oversights in science and IT research. In instances of equal merit, the incorporation of the under-represented sex will be favoured.

Context And Mission

We are seeking a research engineer to join our FPGA and RISC-V architecture teams and contribute to the emulation of RISC-V based designs at FPGA level and other relevant projects.

Key Duties

- Design and develop the necessary hardware or software components
- Conduct research on understanding the state-of-the-art in the related area
- Write reports and do presentations based on project need

Requirements

- Education
  - Bachelor or master degree in computer science or relevant fields

- Essential Knowledge and Professional Experience
  - 0-2 years of experience in FPGA design and RISC-V emulation
  - Deep hands-on experience with FPGAs hardware, software, and toolchain
  - AMD/Xilinx FPGA Toolchain: Vivado, Vitis, SDSOC on Alveo, Versal, or Ultrasclae+
  - Peripheral IPs: DDR and HBM, PCIe, CXL, Ethernet, DMA, UART, nVME, etc
  - Hardware/Software co-design experience: FPGA and Processor
  - HDL and HLS: VHDL, Verilog, SystemVerilog
  - Processor micro-architecture based on risc-v and experience with emulating such designs on FPGAs
  - System software and Operating System flow on FPGA: Linux kernel porting, device drivers, device tree configuration, bootloader configuration (good understanding of Linux Kernel)
  - Debugging and Troubleshooting complex hardware designs (JTAG, ILA, etc) and optimizing the FPGA designs at synthesis, place and route, timing closure, verification, validation

- Competences
  - Self-control
  - Proactive
  - Responsible
  - Quickly adaptable to new topics

Conditions

- The position will be located at BSC within the Computer Sciences Department
- We offer a full-time contract (37.5h/week), a good working environment, a highly stimulating environment with state-of-the-art infrastructure, flexible working hours, extensive training plan, restaurant tickets, private health insurance, support to the relocation procedures
- Duration: Open-ended contract due to technical and scientific activities linked to the project and budget duration
- Holidays: 23 paid vacation days plus 24th and 31st of December per our collective agreement
- Salary: we offer a competitive salary commensurate with the qualifications and experience of the candidate and according to the cost of living in Barcelona
- Starting date: 01/12/2024

Applications procedure and process

All applications must be made through BSC website and contain:

- A full CV in English including contact details
- A Cover Letter with a statement of interest in English, including two contacts for further references - Applications without this document will not be considered

In accordance with the OTM-R principles, a gender-balanced recruitment panel is formed for every vacancy at the beginning of the process. After reviewing the content of the applications, the panel will start the interviews, with at least one technical and one administrative interview. A profile questionnaire as well as a technical exercise may be required during the process.

The panel will make a final decision and all candidates who had contacts with them will receive a feedback with details on the acceptance or rejection of their profile.

At BSC we are seeking continuous improvement in our recruitment processes, for any suggestions or feedback/complaints about our Recruitment Processes, please contact recruitment [at] bsc [dot] es.

For more information follow this link

Deadline

The vacancy will remain open until a suitable candidate has been hired. Applications will be regularly reviewed and potential candidates will be contacted.

OTM-R principles for selection processes

BSC-CNS is committed to the principles of the Code of Conduct for the Recruitment of Researchers of the European Commission and the Open, Transparent and Merit-based Recruitment principles (OTM-R). This is applied for any potential candidate in all our processes, for example by creating gender-balanced recruitment panels and recognizing career breaks etc.
BSC-CNS is an equal opportunity employer committed to diversity and inclusion. We are pleased to consider all qualified applicants for employment without regard to race, color, religion, sex, sexual orientation, gender identity, national origin, age, disability or any other basis protected by applicable state or local law.
For more information follow this link
Barcelona Supercomputing Center - Centro Nacional de Supercomputación

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