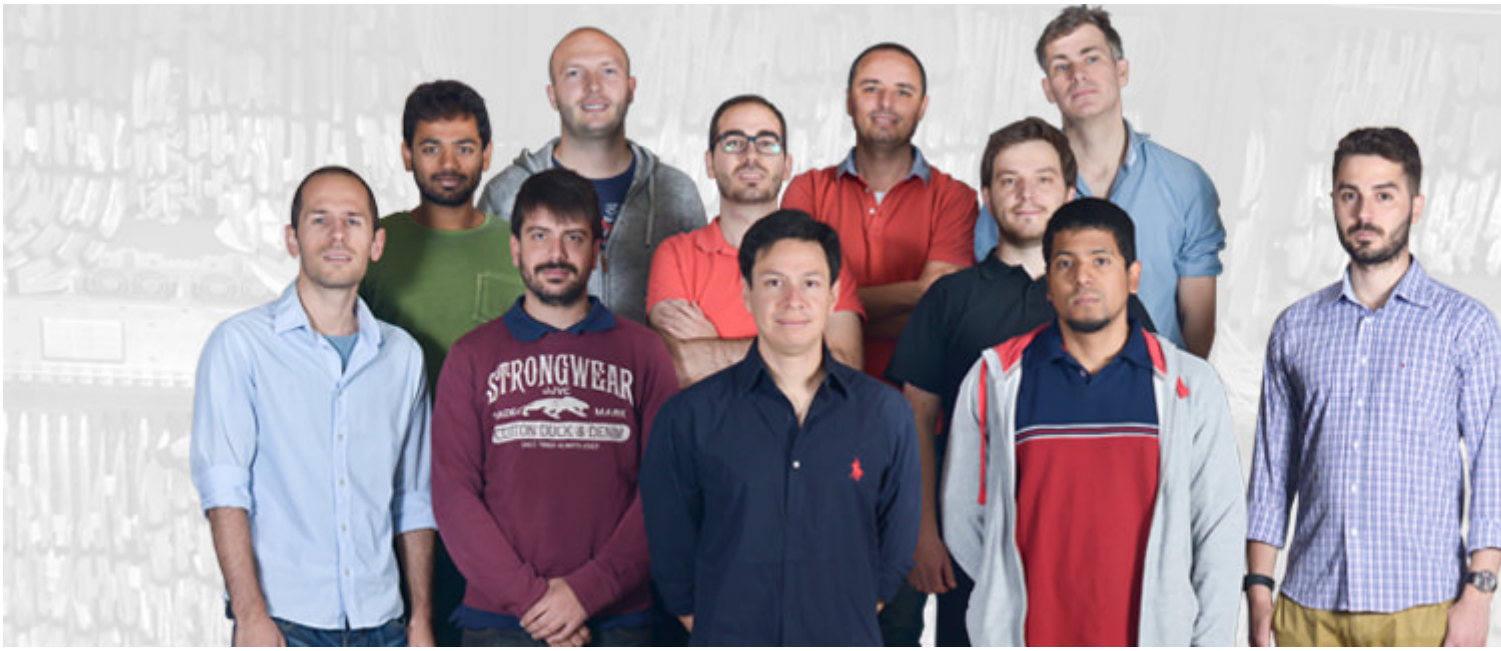
Heterogeneous architectures



Computer Architecture is the design and internal organization of a computer system to meet its requirements, as efficiently as possible, within technology and cost constraints. Simply adding more resources to a computer system does not always make it faster, especially when the main limit is power consumption. Computer architecture addresses all levels of the computer system, from the core, chip, memory, board, to the whole system and its interconnect. Finding the right balance in the design and proposing new design alternatives are key tasks of the computer architect. Currently, our work is focused on the following research areas:

Microserver architectures and system software. We are working at the boundary between microserver system architecture and system software. Our main research lines are intelligent management techniques for interconnect energy proportionality, hypervisor and runtime support for management of shared resources, and performance and energy evaluation of data centre workloads on prototype hardware. This work is currently supported by the FP7 EUROSERVER project.

Memory systems for high-performance computing. The HPC memory systems face many challenges — the memory has to provide higher performance with a limited power budget, while reaching the reliability limits. To address these challenges we characterize the memory requirements of state-of-the-art HPC systems, and identify technology-related features that match these requirements. Also, we detect and analyze DRAM errors of production HPC workloads running on the MareNostrum supercomputer, one of six Tier-0 systems in Europe.

Mobile and embedded-based HPC. As mobile technology is highly integrated, cheap and energy efficient, we explore how to reduce space, money and power using mobile embedded technology in HPC environment. This translates in deploying clusters of ARM-based SoCs equiped with a funcional HPC software stack that we can use in order to explore and extrapolate future HPC architectures. Also we coordinate the Mont-Blanc project, a FP7 European Project involving 12 European industrial and academic partners that evaluate mobile embedded technology for scientific and HPC computation.

Objectives

The Heterogeneous Architectures Group has three main goals:

1. To propose new processor designs that provide higher computing performance at lower energy cost. Research on processor microarchitecture techniques that efficiently exploit different levels of parallelism; either instruction level parallelism (ILP), data level parallelism (DLP), or thread level parallelism (TLP).
2. To understand and overcome the challenges in the design of next-generation memory systems for large-scale HPC clusters.
3. To propose and develop novel design methodologies that enable researchers to explore the huge design space represented by future computer architectures. Research on processor performance prediction models and simulation methodologies for heterogeneous on-chip multiprocessor systems.

Barcelona Supercomputing Center - Centro Nacional de Supercomputación

---